UCD Console for UCD-400



User Manual

/// UNIGRAF



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UCD-400 products meet the essential health and safety requirements, is in conformity with and the CE marking has been applied according to the relevant EU Directives using the relevant section of the corresponding standards and other normative documents.

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1. ABOUT THIS MANUAL

Purpose

This guide is User Manual of UCD-400, USB-connected video interface test unit for use with a PC with Windows® 10 Windows® 8 or Windows® 7 operating system.

The purpose of this guide is to

- Provide an overview of the product and its features.
- Provide instructions for the user on how to install the software and the drivers.
- Provide instructions for the user on how to update the FW of the unit.
- Introduce the HW features of the UCD-400 units.
- Provide instructions for the user on how to use UCD Console software.

Product and Driver Version

This manual explains features found in UCD Console Software Package **1.8.** Please consult Unigraf for differences or upgrades of previous versions.

Please consult the Release Notes document in the installation package for details of the SW and FW versions and changes to previous releases.

Notes

On certain sections of the manual, when important information or notification is given, text is formatted as follows. Please read these notes carefully.

Note

This text is an important note

2. INTRODUCTION

Product Description

UCD-400 is a high speed, USB 3.0 connected video interface test unit. *UCD Console* is the common graphical user interface (GUI) for Unigraf's UCD-400 and UCD-300 family units. The outlook and details of UCD Console will be different depending on the capabilities of the connected unit reflecting the features enabled.

UCD-400 units feature a high-level Software Development Kit (SDK) for use in automated testing. It is called Test Software Interface (TSI). TSI allows for an easy integration of Production and R&D testing routines into an automated test system environment. Please refer to TSI documentation found in additional Unigraf manuals for more details.

Product Features

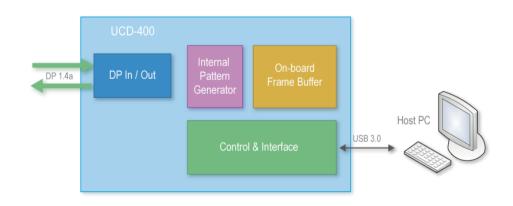
- High resolution video and audio capture up to 8K 30 Hz, 4K / UHD 120 Hz
- Supports HBR3 feature of DP 1.4a
- Compatible with HDCP versions 1.3 and 2.3
- 2 GB on-board high-speed video buffer
- High speed USB 3.0 host PC interface

Please refer to Product Specifications in the appendix of this document for details.

Functional Description

UCD-400 units consist of a multimedia signal input stage, an internal pattern generator, a control stage with on-board frame buffer and a PC interface stage. In the Input Stage the signal is conditioned and converted to desired format. The Interface and Control stages are either passing the captured data directly to the USB interface or storing it to the frame buffer. The internal pattern generator is able to source a signal for testing sink and branch units. The Interface & Control stages are receiving instructions from the host PC to configure and control the functionality of the unit.

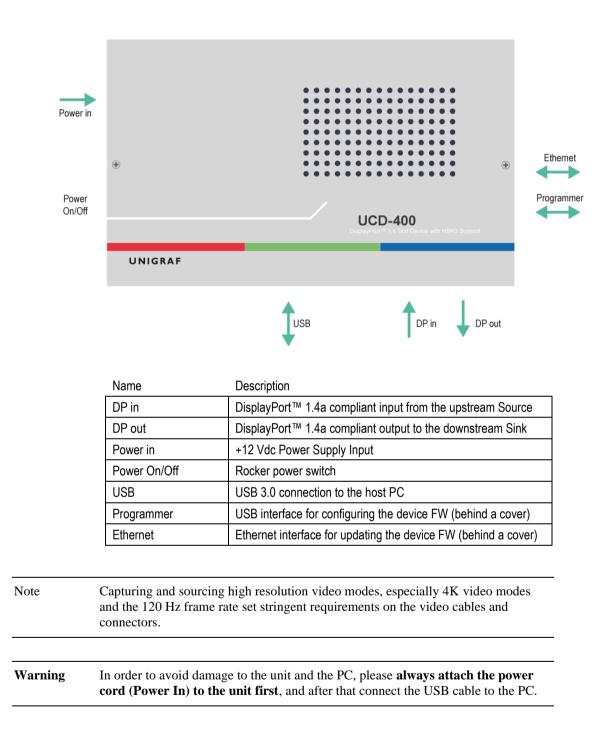
Please find below logical diagram of UCD-400 unit



Introduction

UCD-400

The image below indicates the connections in $UCD\mathchar`-400$ unit and their description.



USB Type-C Interface

UCD-400 delivery package includes a "C to DP Bi-directional Cable" to enable testing of Sink or Source devices with USB-C interface.

Introduction

UNIGRAF

Unpacking

The UCD-400 product shipment contains:

- The UCD-400 unit
- AC/DC Power supply (100 to 240 Vac 50/60 Hz input, +12 Vdc output)
- USB 3.0 compliant cable for host PC connection
- Micro-USB type B compatible cable for FW programming
- USB-C to DP Bi-directional Cable for testing USB-C sinks or sources

Installation Package

The UCD-400 software installation package can be obtained from Unigraf download page at https://www.unigraf.fi/support/download-links. Please log in with the following credentials before attempting to access the download page: Username: *unigraf* Password: *ruukintie*

The installation package is a bundle between the components needed for UCD Console and for TSI SDK. The bundle contains the following items:

- Windows drivers (installed during set up)
- UCD Console software GUI (installed during set up)
- License Manager (installed during set up)
- DSC Test Content and DSC compression tools (optionally installed during set up)
- TSI SDK (optionally installed during set up)
- User Manuals including this document.

In some cases, also the firmware of the unit needs to be updated. If in doubt, please contact Unigraf.

Note:	The software should be installed before connecting the UCD-400 unit in the PC.

Note:

System administrator's privileges are required for performing the installation.

Software Installation

Start the installation by running Unigraf Software Bundle Setup.exe

Once the installer has started, a welcome page is displayed. The welcome page shows the software package release version.

Click Next to continue. The next dialog you need to agree to Unigraf Software End User License and select the components installed.

Note The size of the DSC Content Library is 2.6 Gbytes
--

- Next dialogs define the installation folder in your PC and the Start Menu folder used.
- When the selections are ready, click **Install** to start the installation.
- Click **Finish** to exit the installation dialog.

3. LICENSE MANAGER

Licensing

The features of UCD Console GUI are divided into groups based on the target use of the device. Some basic features can be used without licenses. Advanced feature groups have their dedicated licenses that open the related part of the GUI or enable the related control.

Unigraf licenses are provided as strings of characters, **License Keys**. Each License Key enables a dedicated function in one device. Each device has its dedicated **Seed Number**. Each **License Key** is tied to one **Seed Number**. License Keys can be freely used in any number of PCs

License keys are managed with Unigraf License Manager. By default, shortcut to Unigraf License Manager can be found in Start Menu under: All programs/Unigraf/UCD-400.

Please click **Yes** in the first dialog. License Manager can be run only with Administrator rights.

Note:

System administrator's privileges are required for accessing the licenses.

License Manager GUI

When run, License Manager will list the licensing enabled Unigraf devices. If no suitable device families are detected, License Manager will exit. Please first select one of the available device families by clicking one of the device family selector buttons.

🕖 Unigraf - License Manager					-	×
		Please, Select device fa	mily	-		
		000 000 00000				
	www.unigraf.fi		About version 1.2 [R0]			

In the list of Attached Devices please select the device in question. The *serial number* and the *seed number* of your device are printed in a sticker attached to the bottom of the device.

🕖 Unigraf - License Manager	-		\times
A Back	License management for UCD-1, UCD-	2, UCD-3xx	Devices
Attached Devices:			
UCD-400 [1949C335] SW Emulated device [EMU001]	Select a device to edit licenses		
🚯 Refresh			

The **Back** button opens the device family selection screen. The **Refresh** button will re-scan the system for installed hardware.



Managing Licenses

Seed Number

🧶 Unigraf - License Manager			-		×
d Back		License management for UCD-:	I, UCD-2	, UCD-3xx	Devices
Attached Devices:	Enter new license for device with se	ed number 70b076560100005f:			
UCD-400 [1949C335] SW Emulated device [EMU001]				Insta	.11
	Installed licenses:				
	License	Кеу			
	TSI Advanced Set with HDCP2.2 UCD Pro for DP Sink	33MC-L			
	UCD Pro for DP Sink	68P7-V JH-XJFS 638F-1			
	HDCP 2.2 Support	S9W6-F			
Refresh	Import	Export	×	Remove Se	elected

Each license is tied to a hardware unit with the help of the **Seed Number**. Each unit has a unique Seed Number. Seed Number of the selected unit can be found in the top of the dialog.

Seed Number of the selected device can be copied from dialog link for e.g. ordering Licenses.

Adding New License Keys

To add a new license key for a device, please enter the characters from the license sticker to the boxes provided. The License Manager will automatically move the caret across the edit boxes during typing. If the key is given in text format, copy it and paste to the leftmost box.

Once the license key is fully entered, click the **Install**. The license is authenticated and if it is valid, the license will appear in the list of installed licenses. If the key fails to authenticate, an error message is displayed. If this happens, please make sure that the key has been typed correctly and that the seed number on the license key sticker matches the seed number displayed seed number for the device.

Please note that to avoid confusion, some letters will never appear in a license key because they resemble numbers: For example, capital 'G' and number '6' are very similar when printed with small font. When in doubt, use numbers.

Also, please notice, that characters that can't be part of valid license key are not accepted as input. When appropriate an automatic conversion is applied while typing: For example, lower case letters are converted to upper case automatically.

Managing Installed Licenses

The Installed licenses list shows all currently installed licenses for the currently selected device. The list shows the actual license key, and what that key unlocks.

Remove Selected will uninstall selected licenses. To uninstall a license, click on the license and then click the Remove Selected button.

Export will allow all installed licenses for the currently selected device to be saved into an INI file for backup and distribution to other PCs. To export a license, click on the license and then click the Export button. Please notice that licenses from multiple devices can be exported into the same INI file.

Import will install licenses from an INI file for the currently selected device.

4. FIRMWARE UPDATE PROCEDURE

FW Update Tool

The firmware (FW) of UCD-400 is programmed with a separate tool called **Quartus Prime (includes Nios II EDS)**. The tool can be downloaded from **Intel® FPGA** website:

https://fpgasoftware.intel.com/?edition=lite

On the download page, please **Select release 16.1.** Please download **Quartus Prime** (includes Nios II EDS).

est Release: v19.1	Intel' Quartus' Prime Design Software
ect release: 16.1 • Please select release	2 16.1
erating System 👔 🖓 Windows 🖲 🔬 Linux	
	is available. Users should upgrade to the latest version of the ude the latest open source components that have functiona contact our <u>support team</u> .
You may be exposed to a vulnerability issue if you have rom v11.0 to v18.0 to a location with space(s) in the path.	installed or plan to install Quartus Prime/Quartus II softwa See this <u>KDB solution</u> for more details.
The Quartus Prime Lite software version 16.1 supports IAX II, MAX V, and MAX 10 FPGA. <u>More</u>	the following device families: Arria II, Cyclone IV, Cyclone V
	0
Combined Files Individual Files Additional Sof	itware Updates
Download and install instructions: <u>More</u> Read Intel FPGA Software v16.1 Installation FAQ	
	Updates Available
Read Intel FPGA Software v16.1 Installation FAQ	Updates Available
Read Intel FPGA Software v16.1 Installation FAQ Quick Start Guide	0
Read Intel FPGA Software v16.1 Installation FAQ Quick Start Guide Quartus Prime Lite Edition (Free) Quartus Prime (includes Nios II EDS)	s8019B3CAB62
Read Intel FPGA Software v16.1 Installation FAQ Quick Start Guide Quartus Prime Lite Edition (Free) Quartus Prime (includes Nios II EDS) Size: 2.0 GB MD5: 0FFD781FCC23C6FABC6A6 ModelSim-Intel FPGA Edition (includes Start Size: 1.1 GB MD5: F665D7016FF793E64F57B ** Require 32-bit libraries, see installation manual	s8019B3CAB62
Read Intel FPGA Software v16.1 Installation FAQ Quick Start Guide Quartus Prime Lite Edition (Free) Quartus Prime (includes Nios II EDS) Size: 2.0 GB MD5: 0FFD781FCC23C6FABC6A6 ModelSim-Intel FPGA Edition (includes Start Size: 1.1 GB MD5: F665D7016FF793E64F57B	s8019B3CAB62

Note: Registering is needed for the download.

Please download and install the tool in the PC.

Connect to the UCD-400 Unit

- ▶ Power on the UCD-400.
- Connect UCD-400 with a USB cable to the PC through Programmer connector. (Pls refer to page 7)

The programming interface is the Ethernet connector in the UCD-400 unit. The PC can be connected to the UCD-400 unit either through a network HUB or directly.

Please follow either of the two procedures below.

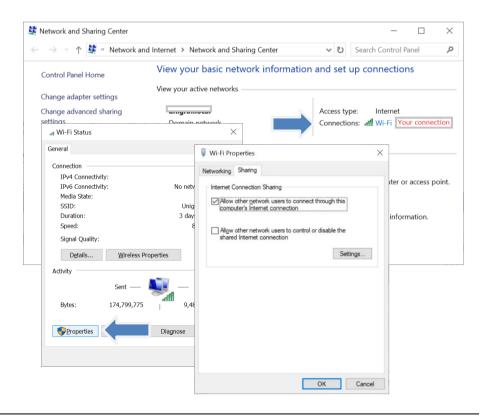
Connecting Through Ethernet Network (Alternative 1)

• Connect UCD-400 though **Ethernet** connector to the same network HUB where the programming PC is connected.

Connecting with Direct Ethernet Cable (Alternative 2)

In case of direct connection, the PC needs to be configured to be an Ethernet network host by enabling WIFI network share (The WIFI network will not be used for programming).

- Connect UCD-400 directly to the PC though **Ethernet** connector;
- Enable **WIFI** Internet access of the PC.
- From Network and Sharing Center click on the WiFi connection
- In Wi-Fi Status dialog click **Properties** and select **Sharing** tab
- Select Allow other network users to connect through this computer's Internet connection
- Click **OK** and **Close**.





The network sharing is shown above for Windows 10. Similar controls can be found for other Windows versions and other operating systems.

Programming the FW

Run Nios II 16.1 Command Shell application as Administrator

Note *Nios II 16.1 Command Shell* application needs to be run as Administrator (Right click with mouse and select **Run as Administrator**)

Select FW update folder location. For example:

cd /cygdrive/c/Program\ Files\ \(x86\)/Unigraf/TSI/UCD-400/Firmware/

Run the boot loader that initiates the HTML programming interface.

source run.sh

Upon command completion, the **assigned IP address for UCD-400 device** is highlighted in the picture below.

/cygdrive/c/Program Files (x86)/Unigraf/TSI/UCD-400/Firmware –	×
jsa@t4405 /cygdrive/c/Program Files (x86)/Unigraf/TSI/UCD-400/Firmware \$ source run.sh Searching for SOF file: in . al0_fpga_bup.sof	^
Warning (210120): Arria 10 information is incomplete. The ISP clamp functionality will be disabled.	
Info: Running Quartus Prime Programmer	
Info: Command; quarts-pageno_bannermode=jtag -o p;a10_fpga_bup.sof Info (213045): Using programming cable "USB-BlasterII [USB-1]"	
Info (213011): Using programming file al@_fpga_bup.sof with checksum 0x30E7799E for device 10ax115s3f45e2sge3@ Info (209060): Started Programmer operation at Mon Jan 20 11:13:25 2020 Info (2090616): Configuring device index 1	
Info (209017): Device 1 contains JTAG ID code 0x02E660DD Info (209007): Configuration succeeded 1 device(s) configured	
Info (200011): Successfully performed operation(s) Info (200061): Ended Programmer operation at Mon Jan 20 11:13:40 2020	
Info: Quartus Prime Programmer was successful. 0 errors, 1 warning	
Info: Peak virtual memory: 5626 megabytes Info: Processing ended: Mon Jan 20 11:13:40 2020	
Info: Elapsed time: 00:00:29 Info: Total CPU time (on all processors): 00:00:16	
Using cable "USB-BlasterII [USB-1]", device 1, instance 0x00 Pausing target processor: OK	
Initializing CPU cache (if present) OK	
Downloaded 411KB in 0.4s (1027.5KB/s) Verified OK	
Waiting to allow other programs to start: done	
Starting processor at address 0x102002BC niss2-terminal: connected to hardware target using JTAG UART on cable	
nios2-terminal: "USB-BlasterII [USB-1]", device 1, instance 0 nios2-terminal: (Use the IDE stop button or Ctrl-C to terminate)	
PHY INFO: [phyid] 0x0 0x141 0xcc2	
PHY INFO: [phyid] 0x0 0x141 0xcc2 InterNiche Portable TCP/IP, v3.1	
Copyright 1996-2008 by InterNiche Technologies. All rights reserved.	
prep_tse_mac 0	
Your Ethernet MAC address is 00:07:ed:2a:09:44	
prepped 1 interface, initializing [tse_mac_init]	
INFO : TSE MAC 0 found at address 0x10003000 INFO : PHY Marvell 88E1111 found at PHY address 0x00 of MAC Group[0]	
INFO : PHY[0.0] - Automatically mapped to tse_mac_device[0] INFO : PHY[0.0] - Restart Auto-Negotiation, checking PHY link	
INFO : PHY[0.0] - Auto-Negotiation PASSED INFO : PCS[0.0] - Configuring PCS operating mode	
INFO : PCS[0.0] - PCS SGMII mode enabled	
INFO : PHY[0.0] - Link established	
INFO : PHY[0.0] - Speed = 1000, Duplex = Full OK, x=0, CMD_CONFIG=0x00000000	
MAC post-initialization: CMD_CONFIG=0x0400020b	
[tse_sgdma_read_init] RX descriptor chain desc (1 depth) created mctest init called	
IP address of et1 : 0.0.0.0 Created "Inst main" task (Prio: 2)	
IP address of et1 : 0.0.0.0 Created "Inet main" task (Prio: 2) Created "Clock tick" task (Prio: 3) Acquired IP address via DHCP clight for interface: et1	
IP address : 194.110.112.79	
Subnet Mask: 255.255.255.0 Gateway : 194.110.112.1	

- Launch web browser on the PC. If Ethernet connection is used, please make sure that the PC is connected to the same network as the UCD-400 unit.
- Access the HTML programming interface by entering the IP address assigned for the UCD-400 unit.

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Most V	Visited 🌙	// /// Login	n - User	Fo	🙏 AdWord	is 🔒	🥂 CC	🗊 Sea	rch Conso	e a	<u>8</u> 🔿	🛈 R	edmine	J D	ata Studio	- 🗊 S	Status		0	
4	ŴП	目で	7°										Arr	ial 1() GX F				ate Po ment	
bc th co fu Up or ac FP <u>Pr</u> In av	oard. This he flash o ontains a unction. W pdate Pool .kits/aru ne examp ccomplish PGA syste roccessor nstruction vailable <u>h</u>	re File Nar	oordinati d and pr ocessor stall the esign are IOAX115 to remote a webse see appli irn more ing your Uploac	ion wi rovide and t devel insta 5SF4 aly up rver, icatio about own	ith the FPGA es links to u the Triple Sp lopment kit alled in the 5_fpga/e s date an FPC and it can a and it can a and it can a sn ote <u>ANA</u> ; ut remote u .sof/.elf fi	A design iseful info beed Eth design f camples GA syste also be u 29: Rem pdate. illes for u to User Softwa	servin formation ernet r files on s/boar ern over used to note Con uploadin Portion are Fil	g it, allow on on the media ac your sys rd_upda r Etherne update j nfiguration ng to flas on of Flas e Name	ws you to a Altera® cess cont stem, the ate_port; at. Remot just the fir pon Over E sh via the ash Mem	write ne website rol (MAC design f al direct e update mware <u>thernet</u> Board L	w FPGA . The FP .) Mega files for t cory. This a can be of anem with the Jpdate P	images GA des Core® the Boa s desigr bedded <i>Nios II</i> Portal ar	sto ign is e	<u>e</u>	Cit Speci Arrial® Develo High-sp Arrial 1 General Board I Licensit Softwa Technic Develo Embed	10 G> pment peed so 0 FPG, Design Design ng re Dow cal Sup pment	(FPGA Kit erial so As Resou nload port C kits	ources ources ource Ce Center enter	nter	
-	Brows	e a10_d	ptrx_p1.	flash.		Brow	/se	No file s	elected.			Upload			Altera	Forum Wiki				
														c)ther Uti	ilities				
			Ν		rial 10 GX										 Factory 	Resto	re			
									ltera Corpo		ll Rights I									

- Browse Hardware File Name for UCD-400 update (e.g. a10_dptrx_p1.flash) and then press "Upload" button
- Once uploading process done cycle power on the UCD-400.

Note Please cycle the power on the UCD-400 unit to enable the FW update.

5. UCD CONSOLE

UCD Console is the graphical user interface (GUI) of UCD-400 for desktop use. It provides the user access to all features of the unit. UCD Console also includes powerful debugging and analysis tools enabling the user to monitor the status of the display interfaces and assist in the problem detection.

The various features of the UCD-400 are divided into interface specific screens and tabs. Each tab contains data and controls for a specific feature.

Device Selection

A shortcut of UCD Console can be found by default under Start Menu path All programs/Unigraf/UCD-400. Once UCD Console GUI is launched the dialog provides a list of UCD-400 devices connected in the PC. Please select the target device by clicking on the appropriate button. If your device cannot be found in the list, please confirm the power and USB connection to the device and click the **Rescan**... button.

///	UCD Co	nsole			-	×
<u>F</u> ile	<u>V</u> iew	<u>T</u> ools	<u>H</u> elp			
Device						
				Select Device UCD-400 [1924C312]		
				🖗 Rescan		
				www.unigraf.fi UCD Console V1.9 [R0], Build# 25582		

Select Role

The use of UCD-400 devices with UCD Console is divided in display interface specific roles. The structure of UCD Console varies between roles by having a varying set of tabs dedicated to functionalities available in the enabled role. The table below lists the roles and tabs available in each role. Please find a detailed description of each role in the later chapters of this manual.

Each UCD-400 model features a unique set of modes available. In special occasions, Unigraf can create custom configurations. Please contact Unigraf Support for details.

Warning about DSC Test Content

When running DSC Compliance Tests, UCD-400 needs to have access to DSC content used as test patterns. The content can be created from the source bitmap files downloaded during installation (optional) either with Unigraf DSC Content Creator or created by the Compliance Test Tool on-the-fly during the compliance test.

Warning	×
	Currently configured DSC test content directory does not contain the source files required to generate missing files, but the auto generate missing files is enabled.
	Please, check the DSC Content settings.
	NOTE: If you did not install the DSC RAW source files or you have the full library available then you should disable auto-generate missing DSC files option from the Options dialog
	ОК

If *Automatically create missing content* is selected in Tools > Options menu, but the source files have not been installed a *Warning* dialog will open. Clicking **OK** will open the *Option* menu.

You can either re-install the whole SW package with DSC Content Library or deselect *Automatically create missing content* in Option menu.

Applying Changes

In various UCD Console dialogues the user needs to update several parameter or fields to make the changes needed. In order to avoid false combinations of parameters the new parameters are applied to UCD-400 only after **Apply** is clicked. In UCD Console the situation that parameters have been changed but not applied is indicated by **bold values** of the parameter.

<i>///</i> U	JCD-400 [1924	C312] - DisplayPort So	urce and Sink				-	
<u>F</u> ile	<u>V</u> iew <u>T</u> ools	<u>H</u> elp						
	Pattern Gene	erator Audio Generator			EC Sink DUT Te	sting		
8	Video Patterr	n Generator					Custom image	
Device	MST	Number of streams 1				^		
Ĕ	VESA 4096	x 2160 @ 60.0Hz	✓ 10 bpc	white	e Vertical Stri	pes 🗸	1995 - 1905 - 19	
RX DP	RGB	\sim	\sim	1	▲ 1	*		
8			 8 bpc 	\sim		\sim		
8	RGB	\sim	\sim	1	× 1	A V		
Event Log			✓ 8 bpc	\sim		\sim		
Ē	RGB		\sim	1	* 1		Default.bmp	

Options

Options can be found in **Tools > Options**.

Video, Audio and Misc options AUX Analyzer options Image File Format PPM BMP JPG Audio File Format WAV Audio Buffer size Main buffer, Ksamples I6 Playback buffer, Ksamples Polders Directory to save images and audio C: Userse ■ ■ ■ ■ ■ ■ Preset directory C: Userse ■ ■ ■ ■ ■ ■ Bit: Browse DSC DSC Work folder C: (Temp\DSC DSC test content directory C: \ProgramData\UnigraflpSC_content_lbrary Automatically created DSC content files Misc. options Apply colour conversion to saved images Bypass 4:2:x -> 4:4:4 conversions Disable firmware version check HDCP protected monitor Misc. options Disable firmware version check HDCP protected monitor Main contention Main contenticon Main contenticon	Options)
○ PPM ○ BMP ● JPG Audio File Format ● WAV Audio Buffer size Main buffer, Ksamples 16 ● Playback buffer, Ksamples 2 Folders Directory to save images and audio ○ (Userse • ■ ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●	Video, Audio and Misc options AUX Analyzer options	
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Disable firmware version check		
	_	
HDCP protected monitor		
	HDCP protected monitor	
	V OK X Cancel	
V OK Cancel		

Video Audio and Misc. Options

Image File Format

You can save the captured frames either in PPM, BMP or JPG bitmap file format. In PPM format the files are stored with the captured color depth, with other formats the color depth is truncated to 8 bits per color.

Audio File Format

Audio files are stored in WAV format

Audio Buffer size

Main buffer: Length of the buffer in the PC memory storing audio samples for monitoring audio format in DP RX / Audio tab. Increased buffer length will enable longer time span to be monitored.

Playback buffer: Length in the buffer in the PC for transferring captured audio to PC sound system. Increased buffer size will ensure a smooth audio output but will also increase the delay between the capture of the audio stream and its playback.

Folders

Please select the directories in the PC for saving the captured images and audio, the saved Presets

DSC

DSC Work folder: Folder for DSC Work files.

DSC test content directory: Folder where DSC source bitmap files, related configuration files and DSC conversion tools are stored.

Automatically create missing content: When selected, compliance test tool During execution of DSC Compliance Tests, the tool automatically creates the DSC compressed content used for testing the DUT.

Keep auto-created DSC content files: By default, the DSC compressed content is deleted after use. If selected, the content is not kept, not deleted.

Warning Keeping the automatically created DSC compressed content will shorten the time needed for running the DSC compliance tests.

Please note, that the space needed for storing the full library **can be very large** (appr. 100 GBytes). Please make sure that the content will be stored in a medium that has the required space available.

Misc. options

Apply color conversions to saved images: When saving captured frames, the Color Mode selected in *Video* tab will be applied also to saved images.

Bypass 4:2:x \rightarrow *4:4:4 conversions*: 4:2:2 and 4:2:0 images are previewed and stored as received, without pixel doubling.

Disable firmware version check: UCD Console lets the user operate a non-matching Software / Firmware combination. NOT RECOMMENDED.

HDCP protected monitor: Text appearing if the monitor where UCD Console is viewed is HDCP compliant and HDCP is enabled. This feature enables preview of captured HDCP encrypted content in *Video* tab.

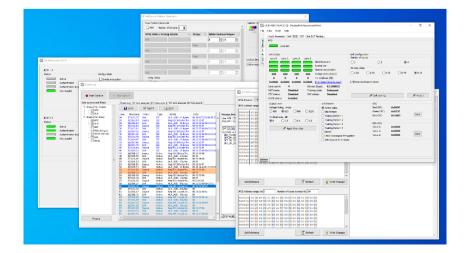
AUX Analyzer Options

Options for configuring the way data is presented in AUX Analyzer tab in Event Log.

Please find full description of the controls in chapter *Event Log / DP AUX Analyzer* later in this document.

Detaching Tabs

Most of the UCD Console tabs can be detached into a separate window for monitoring and controlling separate features simultaneously. To detach a tab **Right-click** on a tab and select **Detach Page**. To glue the tab back to the main window, click on the red **Close button** in the top right-hand corner of the window or press <**Alt**> + **F4** on the keyboard.



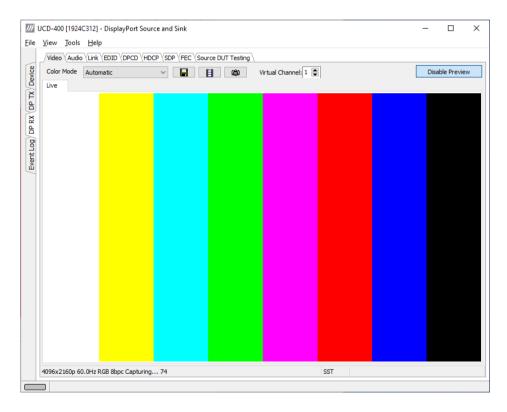
6. DISPLAYPORT REFERENCE SINK

DisplayPort Reference Sink dialog (DP RX) can be selected from the vertical tab on the left edge of the GUI. The horizontal tabs on the top of the GUI enable the various functions available for the input channel. Some of the tabs are enabled by default, some only when an applicable license is included. DPRX features the following functions.

- Video preview and saving (Video)
- Audio monitoring and saving (Audio)
- Status information and control of the upstream link (Link)
- EDID editor (EDID)
- DPCD editor (DPCD)
- HDCP status monitor and control (HDCP)
- SDP sent by the Source device (SDP)
- FEC feature control and status (FEC)
- Source DUT Testing.

Video Tab

Video tab is the Preview window for the captured DisplayPort stream.



Input video mode

7680x4320p 30.0Hz RGB 8bpc Capturing... 76

The measured input resolution, frame rate and color format are shown below the preview window. The indication of the number of frames captured to the PC indicates the pace of the image data transfer to the PC.

Disable / Enable Preview

Click here the button to start or stop capturing video frames.



The top ribbon of the tab has the following controls:

Color Mode for preview

YCbCr (ITU-709) -> RGB ~

- No Conversion: The captured color components are interpreted as R, G and B respectively. No color conversion will be done.
- Automatic: The color mode is selected based on the information in the MSA. If there is no color information available, "No Conversion" is used.
- YCbCr (ITU-709) > RGB: The captured data components are interpreted as Y, Cb, and Cr respectively. Color conversion to RGB is done based on ITU-709 standard.
- SMPTE 170M > RGB: The captured data components are interpreted as Y, U, and V respectively. Color conversion to RGB is done based on SMPTE 170M standard.

Note: Please note that the color mode selection applies to the preview window only. All internal functions use the raw image data as captured from the input channel.

Select Virtual Channel

When Multistreaming (MST) is enabled, the monitored stream can be selected here.

Save one frame



Capture and save one video frame as a bitmap file in the PC. The format and storage location can be selected in Tools > Options pull-down menu. The available bitmap formats are PPM, BMP and JPG.

The selections in Tools > Options menu define if the frame bitmap will be stored as captured from the display interface or if the color mode conversion selected for preview will be applied.

Sequence recording



Clicking the button opens a dialog for definition of number of frames recorded. Buffered mode can also be enabled in this dialog.



In buffered mode, all input frames are captured non-drop until the on-board frame buffer will be full. The dialog also informs the capacity of the buffer with the selected video mode.

In non-buffered mode, only one input frame is buffered at a time. Frames will be skipped if the transfer of the data to the PC is slower than the input data rate.

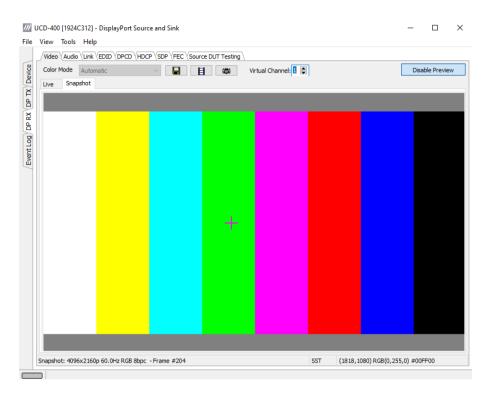
Note: Please note that buffered mode cannot be used when Audio preview is enabled.



Snap preview



When clicked, one frame of the incoming video is captured and shown in a new *Snapshot* tab. The captured bitmap can be saved with **Save one frame** function described above.



Color Information of the Captured Bitmap can be evaluated by placing the mouse cursor on top of the preview image. The lower right-hand side ribbon of the GUI lists

- Location of the cross cursor on the bitmap
- The intensity of the Red, Green and Blue components of the pixel on the cursor location
- The HTML HEX color code of the pixel on cursor location

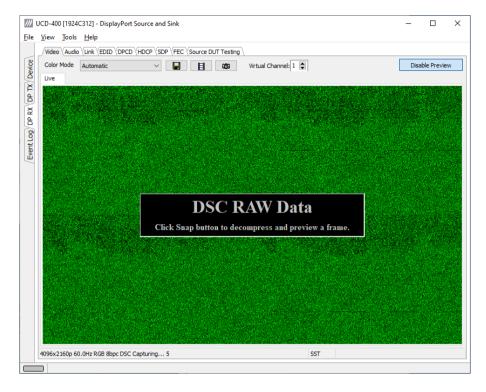
Zoom of the Preview Image can be altered by right clicking on top of the preview image and selecting between

- Fit Window
- Zoom 25%
- Zoom 50%
- Zoom 100%
- Zoom 200%
- Zoom 500%

While in the *Snap preview mode* clicking on the "Camera" icon will take additional snapshots

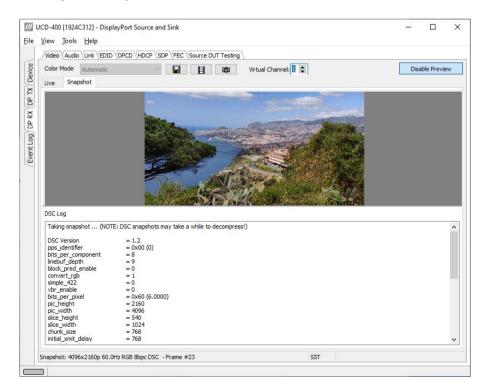
Preview DSC Decompressed Stream

In order to capture and preview DSC compressed video DSC must be enabled by selecting **Link Configuration > Other Capabilities > DSC** checkbox in *Link* tab.



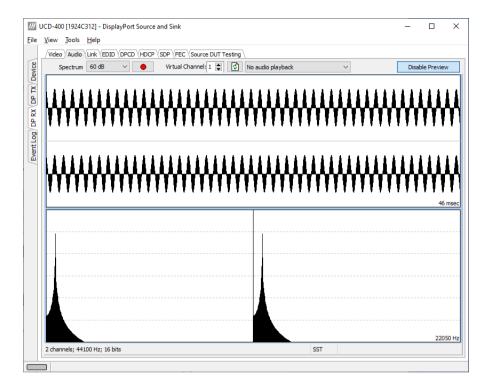
Select Enable Preview to verify that DSC compressed stream is received.

Click **Snap a Frame** button to capture one frame and start the decompressor (offline in the PC). Once the decompression is ready, the frame is shown, and *DSC Log* lists the details of the compressed image.



Audio Tab

Audio tab has a preview of the audio signal format and the controls for audio playback and recording. Up to eight channels will be shown based on the received audio stream.



The audio signal format is shown in three ways

- The 'oscilloscope' panel displays the waveforms of the received audio channels.
- The frequency spectrum of the audio is shown in the lower panel. The range of the spectrum display is from 0 to 1/2 of the input sampling rate. The amplitude scale of the spectrum display can be selected between 'Linear' to 80 dB.
- The horizontal sound level indicator is in the bottom of the dialog.

The span of the preview window is defined with **Audio preview size** found in Tools > Options dialog. The value is given in ksamples (1024 samples). The relation between the preview window span in milliseconds (msec) and the value given in *Audio preview* size depends on the sampling frequency. Please do not exceed the *Audio buffer size* set in the same dialog.

Disable / Enable Preview

This button controls capturing the audio data.

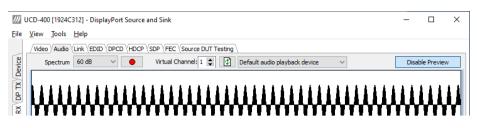
Select Virtual Channel

When Multistreaming (MST) is enabled, the monitored stream can be selected here.



Playback device selection

The captured audio can be played back in the PC. The combo-box defines the audio device in the host PC through which the captured audio is played. By default, the *No audio playback* is chosen.



Note

Please note that the audio capabilities of the audio playback device of the PC are not automatically reflected in the audio capabilities description in UCD-400 EDID. Since UCD-400 is not performing any audio format conversion, it might occur that the source provides an audio format that the selected playback device is not supporting. In case a conflict occurs, please change manually the EDID content or disable audio playback to monitor the waveforms in UCD Console.

Refresh audio device list



Click here to re-read the list of audio devices after making changes to the host PC configuration.

Audio Buffer Size

The amount of buffering used in the data transfer between the UCD-400 unit and the PC in **Audio buffer size** in Tools > Options dialog. Increased buffer size will ensure a smooth audio output but will also increase the delay between the capture of the audio stream and its playback.

Start audio recording



The captured audio can be recorded in the PC using Waveform Audio File Format, WAV (*.wav) format. The pop-up dialog defines recording duration. The folder where the audio file will be saved can be selected in File > Options.

Recording			×
Recording duration, msec:	5000	🗸 ОК	X Cancel

Input audio mode

2 channels; 48000 Hz; 16 bits

This field (in the bottom of the dialog) indicates detected audio mode in the input stream.

Link Tab

Link tab contains four panels: Cable / HPD, Link Status, Link Configuration and Stream Status.

Cable / HPD		PCD (HDCP (S	DP \FEC \So	urce DUT Testing			
	Cable	HPD	🗸 Assert	🚫 Deasser	t 🥖 Pulse HPD	500 🔺 Length,	msec 🧳 Short Pu
Link Status					Link Configuration		
Lane 0	Lane 1 Lane	2 Lane 3			Max Lanes	0.1	0.1
			Clock Recov	ery	01	○ 2	• 4
			Symbol lock Channel equ	alization	Max Bitrate, Gbps	-	
600	600 60	0 600	Voltage swin		0 1.62 0 2.7	0 🔿 5.40	○ 6.75
0	0 0	0	Pre-emphasi		Other Capabilities		
0x0000	0x0000 0x00	-		(Click to clear)	MST TPS3	🗹 TPS4 🗹	FEC DSC
Lane count:	4	Bit rat	e (Gbps): 4	8.1 (HBR3)	Enable fast LT	Force cable st	tatus to plugged
MST mode:	Disabled	l Framin	ig mode: I	Enhanced			
FEC status:			tatus:	Disabled	Generate HPD pulse	e on Apply	🗸 Apply
HDCP statu	s: Disabled		tatus:	Disabled	Generate HPD puise	e on Apply	V Apply
	s: Disabled		tatus: I	Disabled	Generate HPD puise	e on Apply	•
HDCP statu	s: Disabled		tatus: I	Disabled	Generate HPD puise	e on Apply	Update Link Status
HDCP statu: Scrambling:	s: Disabled Enabled		tatus: I	Disabled	∑ Generate HPD puise	e on Apply	-
HDCP statu Scrambling: Stream Sta	s: Disabled Enabled		tatus: I		Generate HPD puise		2 Update Link Status
HDCP statu: Scrambling:	s: Disabled Enabled		1125	Misc		CRC Red: 0x869E	Update Link Status
HDCP statu Scrambling: Stream Sta Horizontal	s: Disabled Enabled	Vertical				CRC	DSC CRC Value 0: -
HDCP statu Scrambling: Stream Sta Horizontal Total:	s: Disabled Enabled itus 2200	Vertical Total:	1125	Misc Frame Rate, Hz	59.995	-CRC Red: 0xB69E	Update Link Status DSC CRC Value 0: - Value 0: - Value 1: -
HDCP statu Scrambling: Stream Sta Horizontal Total: Start:	s: Disabled Enabled Itus 2200 192 1920	Vertical Total: Start:	1125 41 1080	Misc Frame Rate, Hz: Color Depth: Color Encoding:	59.995	CRC Red: 0x8696 Green: 0x833E	Update Link Status DSC CRC Value 0: - Value 0: - Value 1: -

Cable / HPD

Indicator lights of the state of the cable. **Cable** indicates that the hardware has detected an upstream cable. **HPD** indicates that the HPD signal is Asserted (logical "high").

Clicking the **Deassert** button will cause HPD line to be set to logical "low" (de-asserted) and hence no HPD pulse can be generated. Click the **Assert** to re-activate the HPD line (set to logical "high").

To apply an HPD Pulse with programmable duration click **Pulse HPD**. The duration will be defined in the provided field.

For applying a short pulse click Short Pulse. Pulse duration is 1 ms.

Link Status

Link Status displays the status of the link training and the link parameters negotiated between UCD-400 Sink and the Upstream Source. The data is retrieved from the DPCD registers of the UCD-400 Sink. The status is updated automatically.

Link Configuration

Link Configuration allows the user to change the way the Sink capabilities are announced in the DPCD registers of the UCD-400 Sink. Maximum Lane Count and Maximum Link Rate are set with their appropriate radio buttons. To update the new status to the DPCD registers click **Apply**.

Other Capabilities section includes controls of features like MST, FEC and DSC

When **Force cable status to plugged** is checked, sink functionality is active regardless of a failure of upstream device detection e.g. due to incorrect AUX Channel electrical termination.

To apply a Hot-Plug Detect pulse automatically after updating the status, select **Generate HPD pulse on Apply**. HPD pulse duration will be defined in the *Pulse* HPD field.



Stream Status

Stream status is enabled with UCD Pro for DP Sink license.

Video Timing Details are retrieved from the Main-Stream Attributes (MSA) of the monitored stream. Frame rate is measured by UCD-400 Local Sink.

Note: Please note that the MSA information used for Video Timing Details is provided by the Upstream Source, it is not measured by the UCD-400 Local Sink.

CRC

The 16-bit **CRC** (checksum, cyclic redundancy check) values of the three color components calculated by the Sink hardware. To re-calculate, click **Update Link Status**.

The 16-bit **DSC CRC** values of the captured DSC compressed frame. "**Value 0**" is calculated from 1st, 4th, 7th ... byte, "**Value 1**" from 2nd, 5th, 8th ... byte and "**Value 2**" from 3rd, 6th, 9th ... byte.

Multistreaming

When Multistreaming (MST) is enabled and the source sends a multi-stream signal the details of the received virtual channels is shown in a table in *Stream Status* field.

	Audio / Link		PCD HE	CP SD	P (FEC (S	ource DU	T Testing	\											
Cable / I	HPD Cable		🗖 нро	,	🗸 Asser	t	🚫 Dea:	Deassert Pulse HPD 500 + Length, msec Short Pu											
Link Sta	itus							Link Co	nfigura	tion									
Lane () Lane	1 Lane	2 Lar	ne 3				Max La	anes										
				-	Clock Reco	very		01			O 2		0 4						
					Symbol loc			Max Bi	trate, (Sbps									
					Channel eo			0 1.6	2	02.70	0	5.40	6.75	• 8.1	0				
400	400				/oltage sw Pre-empha)	Other	Capabi	ities									
3.5 0x000		3.5 00 0x00			re-empna Error Coun		(lear)	MST	г	TPS3	TPS4	FE	c 🗆 🛛	SC					
Lane co		4		Bit rate		8.1 (HB		Ena					us to plugge						
MST mo		Enabled		Framing		Enhanc			idle tas	t L I	Force	e cable stati	us to plugge	a					
FEC sta	tus:	Enabled		DSC sta		Disable	d	Ger Ger	nerate I	HPD pulse	on Apply			🞸 Apply					
HDCP s	tatus:	Enabled																	
Scrambl	Scrambling: Enabled											লি 🗤	date Link St	to the sec					
Scrambl	ing:	Enabled													atus				
	-														latus				
Monito	red virtual	channel:		ream #0		~		ate, Hz: 60.0											
Monito H-Total	red virtual H-Start	channel: H-Active	H-Sync	V-Total	V-Start	V-Active	V-Sync	CEF	BPC	Port #	Stream ID	Req. PBN	Alloc. PBN	First slot	Slot n				
Monito	red virtual	channel: H-Active 4096	H-Sync (+) 88		V-Start 82 41		V-Sync (+) 10	CEF RGB unsp. (k	BPC 8	Port # 0	Stream ID 1	Req. PBN 2125 532			Slot n 36 9				
Monito H-Total 4400	red virtual H-Start 216	channel: H-Active 4096 1920	H-Sync (+) 88	V-Total 2250	82	V-Active 2160	V-Sync	CEF	BPC 8 8	0	1	2125	Alloc. PBN 2160	First slot	Slot n 36				
Monito H-Total 4400 2200	red virtual H-Start 216 192	channel: H-Active 4096 1920 1920	H-Sync (+) 88 (+) 44 (+) 44	V-Total 2250 1125	82 41	V-Active 2160 1080	V-Sync (+) 10 (+) 5	CEF RGB unsp. (k RGB unsp. (k	BPC 8 8 8	0	1 2	2125 532	Alloc. PBN 2160 540	First slot 1 37	Slot n 36 9				

EDID Tab

EDID Tab provides tools for accessing the EDID of the UCD-400 Sink presented to the Upstream Source Device. There are three basic functions:

- Load and save EDID data files in the host PC
- Edit the EDID contents
- Program and read the contents of the EDID memory of up to four virtual MST Ports

<i>///</i> (UCD-400 [1924C312] - DisplayPort Source and Sink		- 🗆 X
<u>F</u> ile	<u>V</u> iew <u>T</u> ools <u>H</u> elp		
	/Video \Audio \Link \EDID \DPCD \HDCP \SDP \FEC \Source DUT Testing \		
8	EDID Data:		EDID Files
Device	000000 00 ff ff ff ff ff ff 00 54 c7 36 40 4c 34 32 30	^	EDID Files
Ĩ	000010 34 18 01 04 e5 3d 23 78 3a 5f b1 a2 57 4f a2 28		Load
8	000020 0f 50 54 bf ef 80 71 4f 81 00 81 c0 81 80 a9 c0 000030 b3 00 95 00 d1 c0 4d d0 00 a0 f0 70 3e 80 30 20		Save as
X	000040 35 00 5f 59 21 00 00 1a 56 5e 00 a0 a0 a0 29 50		Save as
B	000050 30 20 35 00 5f 59 21 00 00 1a 00 00 00 fd 00 38		
8	000060 4b 1e 86 36 00 0a 20 20 20 20 20 20 00 00 00 fc 000070 00 55 43 44 2d 34 30 30 20 44 50 31 0a 20 01 de		HEX Editor
Event Log	000080 02 03 12 71 83 4f 00 00 29 0f 7f 07 15 06 55 3d		
Å	000090 1f c0 00 00 00 00 00 00 00 00 00 00 00 00		Clear
			Append file
	0000c0 00 00 00 00 00 00 00 00 00 00 00		
	0000d0 00 00 00 00 00 00 00 00 00 00 00		EDID Editor
	0000f0 00 00 00 00 00 00 00 00 00 00 00		EDID Editor
			Virtual Channel
			Sink EDID
			Read
		~	Write
		_	-

EDID Files

Note

With **Load...** and **Save as...** a hex EDID file can be read and written from the PC. Please note that the program does not alter the contents of the EDID file or verify its integrity during load and save operation.

Four blocks (512 bytes) of EDID code is read. If the device is not supporting all four blocks, the non-supported area is replaced with zeroes.

Currently the EDID Editor does not support Display ID. Hex EDID files can however be modified with the HEX Editor or externally generated hex EDID files that have Display ID content can be load and programmed into the hardware.

HEX Editor

When EDID content is either loaded from a file or read from the hardware EDID memory, it is shown in the *EDID Data* panel on the left hand side of the dialog. EDID contents can be edited by typing over the existing values. Altered content is highlighted with **RED**. Please note that Hex Editor itself does not alter the contents of the EDID data or verify its integrity.

After editing the data can either be saved to an *.ecd file in the PC with **Save as...** or programmed it to the hardware EDID memory with **Write**.



EDID Editor

EDID Editor is launched in a separate pop-up window. Please see the description of the EDID editor in Chapter <u>EDID Editor</u> later in this document.

✓ Collection 1	Details of ":/0/Version/18-Byte data blocks/	Descriptor 1"	
Blocks in collection	Current Value = Detailed Timing Descripto		
 Block 0 [VESA EDID] 			
Checksum	New Value:		
✓ · Version	Detailed Timing Descriptor		~
Extension flag Vendor & Product ID Basic Display Parameters and F Display x,y Chromacity coordin			
 Established timings I and II 	Details of 1/0/version/10 byte data blocks/		
> Manufacturer's Timings	Key	Value	^
> Standard Timings	Pixel Clock	533250	
✓ 18-Byte data blocks	Horizontal addressable video	3840	
> Descriptor 1	Horizontal Blanking	160	
> Descriptor 2	Vertical addressable video	2160	
> · Descriptor 3	Vertical blanking	62	
> · Descriptor 4 • · Block 1 [CEA 861]	Horizontal Front Porch	48	
- Checksum	Horizontal pulse width	32	
 CEA Extensions Version 	Vertical Front Porch	3	
···· Sink Underscans IT video	Vertical pulse width	5	
Basic audio	Horizontal Video Size	607	
< YCbCr (4:4:4)	Vertical Video Size	345	
· /	a second and a second s	-	*

DPCD Tab

	itor (Audio Generati	or \Link \EDID \DPCD	HDCP FEC Sink E	UT Testing \		
DPCD Decoder	1.4 + DETAILED_CA	P_INFO_AVAIL = 0	~		🔁 Load	Save
DPCD Address ra	inge: 0x 0	Number of bytes to r	read: 0x 100			
000010 00 000020 00 000030 2d 000050 00 000050 00 000050 00 000060 00 000080 00 000080 00 000080 00 000080 00	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	~	Lünk/Sink Device Status SINK-COUNT [RO] 0x00200 := 0x41 SINK_COUNT = 1 CP_READY = 1	
0000d0 00 Set Refer		00 00 00 00 00 0	00 00 00 00 00 Refresh	V Write Changes		
DPCD Address ra	unge: 0x 200	Number of bytes to r		7	-	
	-	11 11 00 00 00 0		^		
000210 00 000220 00 000230 00	80 00 80 00 80 00 00 00 00 00 00 00 00 00 00	00 80 00 00 00 0 00 00 00 00 00 0 00 00 00 0	00 00 00 00 00 00 00 00 00 00 00 00 00 0			
000250 00	00 00 00 00 00	27 00 00 00 00 0 00 00 00 00 00 0 00 00 00	00 00 00 00 00			
000270 00		00 00 00 00 00 00				

DPCD tab is a tool for monitoring and editing the DPCD registers of the UCD-400 Sink.

The tool consists of two independent monitoring and editing windows for the DPCD data. The user can freely select the the DPCD address areas shown on each panel.

The *DPCD Decoder* panel on the right hand side shows the interpretation of the DPCD byte selected on the monitoring windows. The selected byte is shown with a green outline.

The combo box above the DPCD Decoder window allows selection of how the DPCD data is interpreted. It can be either as DP 1.4 DPCD, or as DP 1.4 DPCD with Detailed Capability Info selected or not (DETAILED_CAP_INFO_AVAIL = 1/0).

Click **Refresh** to re-read the data from the DPCD registers to the window in question.

Click **Write Changes** to write the portion of data shown in the window in question to the DPCD registers.

Click Set Reference to store currently shown data as a reference for comparison.

When the data is *Refreshed* from the DPCD registers the changed bytes will be highlighted with gray background.

The fields edited by the user will be highligted with **red** color.

DPCD Decoder 1.4 + DETAILED_CAP_INFO_AVAIL = 0 DPCD Address range: 0x0 Number of bytes to read: 0x 100 000000 14 1 e e4 81 01 00 01 80 00 00 60 00 00 00 00 00 00 00 00 00 00	
$\begin{array}{c} 000000 \\ 000010 \\ 000010 \\ 000010 \\ 000010 \\ 000010 \\ 000010 \\ 000010 \\ 000000 \\ 000000 \\ 000000 \\ 000000 \\ 000000$	LANED_1_STATUS [RO] 0x0002 := 0x77 LANED_CR_DONE = 1 LANED_CR_DONE = 1 LANED_STMBOL_LOCKED = 1 LANE1_CR_DONE = 1 LANE1_CR_DONE = 1 LANE1_STMBOL_LOCKED = 1
000010 00 00 00 00 00 00 00 00 00 00 00 00 00	LANED_1_STATUS [RO] 0x0002 := 0x77 LANED_CR_DONE = 1 LANED_CR_DONE = 1 LANED_STMBOL_LOCKED = 1 LANE1_CR_DONE = 1 LANE1_CR_DONE = 1 LANE1_STMBOL_LOCKED = 1
Set Reference	Write Changes
DPCD Address range: 0x 200 Number of bytes to read: 0x 100	
$\begin{array}{c} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 &$	
	Y

Saving and Loading DPCD Content

DPCD data in the selected address areas can be saved as a file in your PC. There are three alternative formats:

- Binary *DPCD Fata File* format (*.DPD). This is Unigraf proprietary format. You can also load the DPCD content stored in this format.
- Comma Separated Values (*.CSV) for loading the data to a spreadsheet.
- *HEX Dump* (*.HEX) in a human readable text format.
- Click **Save** to select the location and the format of the file.
- Click **Load** to load DPCD data saved in *DPCD Data File* (*.DPD) format to the editor.
- ► To program the data into the DPCD registers of UCD-400 Local Sink click Write Changes.

potentially affect the status and capal	egisters of the UCD-400 Local Sink will
source.	bilities of UCD-400 as seen by the upstream
- User control like Link Training or r	mode changes will modify the content of the
DPCD registers	PCD registers will be returned to their default

HDCP Tab

HDCP tab is the dialog for monitoring the HDCP (for *High-Bandwith Digital Content Protection*) status and controlling the HDCP capabilities of the UCD-400 device.

'''	UCD-400 [19240	2312] - DisplayPort Source and Si	nk	_	×
<u>F</u> ile	<u>V</u> iew <u>T</u> ools	Help			
	/Video Audio		FEC Source DUT Testing		
Event Log/ DP RX DP TX Device	HDCP 1.3 Status	Active Authenticated	Configuration IHDCP Capable Keys Production Facsimile - Trest* None		
Eve	HDCP 2.3 Status	Active Authenticated Dedared as HDCP capable Keys loaded	Configuration HDCP Capable Keys Production		
			ONone		

Status

The status field indicates the HDCP status of the UCD-400 device.

Active: The link between UCD-400 and the upstream source has been encrypted.

Authenticated: The HDCP handshake between the UCD-400 and the sink unit has been completed successfully.

Declared as HDCP capable: The UCD-400 unit recognizes HDCP handshake messages.

Keys loaded: The HDCP keys are loaded to the UCD-400 unit.

Configuration

HDCP Capable: To disable HDCP uncheck the box.

Keys

Select between Production or Facsimile HDCP keys. To remove the keys, select None.

HDCP 1.3 vs. HDCP 2.3

UCD-400 devices support by default both HDCP 1.3 and HDCP 2.3 standard.

SDP Tab

SDP Tab is enabled with UCD Pro for DP Sink license.

In SDP Tab shows the *Secondary-Data Packets* sent by the Source device. Click **Update** to re-read the data.

	JCD-40 <u>V</u> iew				play	/Por	t So	urce	anc	l Sin	k																				-				×
Luc		Aud				DPCE) (H	IDCF	SD	P (F	EC	Sour	ce D	ит т	estir	ng \																			
8	SDP																																		
P TX Device		ACR AIF					0	0 0	2 3	00		08			00		00	00	00	08	00	00	80	00	19 00	00	80	00	00	00	80	00	00	28 00	29 80
			 	10																															
	<																																		>
																																I	Upda	te	

SDP Tab displays in hexadecimal format the following received SDP packets:

- Audio_TimeStamp
- Audio_Stream
- Extension
- Audio_CopyManagement
- ISRC
- Video Stream Configuration (VSC)
- Camera Generic 0
- Camera Generic 1
- Camera Generic 2
- Camera Generic 3
- Camera Generic 4
- Camera Generic 5
- Camera Generic 6
- Camera Generic 7
- Vendor-Specific Infoframe packet
- AVI InfoFrame packet
- Source Product Descriptor InfoFrame packet
- Audio InfoFrame packet
- MPEG Source InfoFrame packet
- Dynamic Range and Mastering InfoFrame
- Picture Parameter Set (PPS)

FEC Tab

FEC Tab is enabled as a basic feature.

FEC tab contains control of the FEC (Forward Error Correction) feature, Error Detection table and FEC Status Log.

e	CD-400 [1924C312] - Displa <u>V</u> iew <u>T</u> ools <u>H</u> elp								
	Video (Audio (Link (EDID (DPCD (HDCP (SDP) FEC (Source DUT Testing)								
3	FEC Capable Generate HPD on change FEC Enabled Fror Counters (DPCD)				FEC Enabled	FEC Status Log			
Š.					Enabled, ready				
		Lane #0	Lane #1						
	Uncorrected block errors		0	0	0				
	Corrected block errors	0	0	0	0				
	Bit errors	0	0		0				
	Parity block errors	0	0	0	0				
	Parity bit errors	0	0	0	0				
	ित्रम	pdate		Thear of the team of team	ounters				
	E 9	public			ounters				
	Charles								
	FEC Status: Decode Enable D					Clea	ar log		

Enabling FEC

Enabling FEC feature is controlled by the source device. When connected, source verifies corresponding registers in sink DPCD to find out if sink is FEC capable. This register in UCD-400 sink can be controlled by **FEC Capable** checkbox.

Since source normally polls sink DPCD mainly after a new connection, selecting **Generate HPD on change** will force a new connection after the change of the FEC capability status.

- Click **Update** to read the FEC Error Counters
- Click **Clear** to clear the counters.

FEC Status Log lists FEC events.

Source DUT Testing Tab

Source DUT Testing Tab is enabled with UCD Pro for DP Sink license.

Please refer to Appendix E later in this document for description of the tests available.

UCD-400 [1924C312] - DisplayPort Source and Sink <u>V</u> iew Iools <u>H</u> elp		_		×
/Video \Audio \Link \EDID \DPCD \HDCP \SDP \FEC \Source DUT Testing				
/ Link-Layer Tests / HDCP 2.3 1A tests / HDCP 2.3 1B tests / HDCP 2.3 3A tests / HDCP 2.3 3B tests / CRC tests	Simple L	T tests	٦.	
Test Name	Pass	Fail	Skip	Run
✓ 1A-01 Regular Procedure - With previously connected Receiver (With stored km)	1	0	0	1
✓ 1A-02 Regular Procedure - With newly connected Receiver (Without stored km)	1	0	0	1
✓ 1A-03 Regular Procedure - Receiver disconnect after AKE_Init	1	0	0	1
✔ 1A-04 Regular Procedure - Receiver disconnect after km	1	0	0	1
 IA-04 Regular Procedure - Receiver disconnect after km IA-05 Regular Procedure - Receiver disconnect after locality check IA-06 Remiter Decedure - Receiver disconnect after locality check 	0	0	0	0
 1A-06 Regular Procedure - Receiver disconnect after ks 	0	0	0	0
 1A-07 Regular Procedure - Receiver sends REAUTH_REQ after Ks 	0	0	0	0
- 1A-08 Irregular Procedure - Verify Receiver Certificate	0	0	0	0
- 1A-09 Irregular Procedure - SRM	0	0	0	0
1A-10 Irregular Procedure - Invalid H'	0	0	0	0
 1A-11 Irregular Procedure - Pairing Failure 	0	0	0	0
- 1A-12 Irregular Procedure - Locality Failure	0	0	0	0
달 Configure [1]	Import	Ľ) E	kport
Run Selected Stop on Failure Repeats: 1 📥 Delay time, sec: 1 🛓 Save Report			Clear /	All
Test Log:				
0002.454.648: [TE-Snk] STEP 1A-04-1 0002.553.541: [TZ-Snk] WARNING. DUT sends unencrypted video 0002.653.675: [TZ-Snk] DUT initiates authentication by transmitting AKE_Init 0002.554.081: Test PASSED: "1A-04 Regular Procedure - Receiver disconnect after km" *** Test complete PASSED ***				,

Select the tests for execution by clicking the corresponding row.

Clicking **Configure...** opens a dialog for defining the test parameters for that set. Please refer to *Test Parameters* below for description.

Parameters from *Test descriptor files* can be loaded with **Import** and stored with **Export**. Please refer to documentation of TSI software API for description.

Tests are started by clicking Run Selected. By clicking Abort the sequence is stopped.

Test flow can be controlled with **Repeats** of the test sequence, **Delay time** between individual tests or **Stop on Failure** that stops the whole sequence if one of the tests fail.

At the completion of each test the result of the test is indicated in the matrix on the right hand side of the test panel. For each test the matrix lists the number of occurrences of each result and the number of tries performed.

Click **Save Report** to generate a HTML report file for sharing the results with other parties for viewing without UCD Console.

By clicking Clear All the test log and the results matrix are cleared.

Test Parameters

Each test set has its dedicated set of test parameters. Open a dialog for defining the parameters by clicking **Configure...**

Parameters of Link Layer CTS

Link Layer CTS parameters includes DUT capabilities defined in *Source Device Capability Question List* in document *DisplayPort Link Layer Compliance Test Specification*. The capabilities are grouped into tabs based on the tested feature.

DP 1.4 LL CTS DUT Source Capabilities							×
General Audio DSC							
Common DSC Version 1.2	Video modes to be tested	to be tested Debug Link Configuration					
DCS Maximum supported slice 24		CTA	RB1	RB2	Lane count:	Bit rate:	
DSC supported	1920 x 1080 @ 30 Hz	\checkmark	\checkmark	\checkmark	1 Lane \sim	RBR (1.62 Gbps) $$	
DSC block prediction supported	1920 x 1080 @ 60 Hz	\checkmark	\checkmark	\checkmark	1 Lane 🔍 🖂	RBR (1.62 Gbps) 🛛 🗸	
Colorimetry	1920 x 1080 @ 120 Hz	\checkmark	\checkmark		4 Lanes 🛛 🗸	RBR (1.62 Gbps) \sim	
RGB	3840 x 2160 @ 30 Hz	\checkmark	\checkmark	\checkmark	4 Lanes \sim	RBR (1.62 Gbps) 🛛 🗸	
8bpc VESA	3840 x 2160 @ 60 Hz	\checkmark	\checkmark	\checkmark	4 Lanes \sim	RBR (1.62 Gbps) 🛛 🗸	
10bpc VESA	3840 x 2160 @ 120 Hz	\checkmark	\checkmark		4 Lanes 🔍 🗸	HBR2 (5.4 Gbps) 🛛 🗸	
12bpc VESA	5120 x 2160 @ 30 Hz	\checkmark	\checkmark	\checkmark	4 Lanes 🔍	RBR (1.62 Gbps) 🛛 🗸	
YCbCr 4:4:4	5120 x 2160 @ 60 Hz	\checkmark	\checkmark		4 Lanes 🔍 🗸	HBR (2.7 Gbps) 🛛 🗸	
Bbpc CTA (ITU. 709)	5120 x 2160 @ 120 Hz	\checkmark	\checkmark		4 Lanes \sim	HBR2 (5.4 Gbps) 🛛 🗸	
10bpc CTA (ITU.709)	7680 x 4320 @ 30 Hz	\checkmark	\checkmark	\checkmark	4 Lanes 🔍	HBR (2.7 Gbps) 🛛 🗸	
12bpc CTA (ITU. 709)	7680 x 4320 @ 60 Hz				4 Lanes 🔍	HBR2 (5.4 Gbps) 🗸	
YCbCr 4:2:2 Simple Bbpc CTA (ITU.709) Bbpc CTA (ITU.709)	7680 x 4320 @ 100 Hz				4 Lanes 🔍	HBR3 (8.10 Gbps) 🖂	
10bpc CTA (ITU.709)		Set / Clear all Enable					
12bpc CTA (ITU.709)							
YCbCr 4:2:0							
8bpc CTA (ITU. 709)							
10bpc CTA (ITU. 709)							
12bpc CTA (ITU. 709)							
Select All							
				_			
Presets					🗸 ок	🗶 Cance	1

Parameters of CRC Test Set

CRC Video test parameters dialog contains fields for defining the test duration, number of frames captured, errors allowed and expected video format.

CRC Video test parameters				\times
Base parameters			Reference CRC's	
Test timeout (milliseconds):	10000	* *		^
Run until timeout			0x3F3A, 0x967D, 0xA7BF 0x3F3A, 0x967D, 0xA7BF	
Test length (# frames):	2000	* *		
Errors allowed (# frames):	20	* *		
Repeat "Continuous motion picture t	est" until timeout			
Test iterations (# of repeats):	1	A		
Expected Video Signal				
Width (# pixels):	4096	▲ ▼		
Height (# pixels):	2160	•		
Reference BPP:	24 BPP	\sim		
Frame rate checking				
Enable frame rate check				~
Expected frame rate (mHz):	60000	×.	CRC Capture length (# frames)	
Frame rate tolerance (±mHz):	100	×	3 Capture now	
Presets			VOK X Cancel	

Click **Capture now** to record *Reference CRCs*. Please define the number of frames used as reference – either one or the number of frames in the predefined test sequence.



Parameters of DP RX Simple LT Tests

The parameters for DP RX Simple LT test set is a subset of DUT capabilities.

Test timeout, milliseconds	5000		
Max lanes count supported by DUT	4		
Max lane rate supported by DUT in 0.27Gbps	20		
Reserved for DUT Capabilities flags	0		
Reserved for DUT Test automation capabilities flags	0		
Long HPD pulse duration, milliseconds	1000		
Link training start timeout, milliseconds	5000		
Delay between test cycles, miliseconds	3000		

Presets

In all parameter dialogs the selected parameters can be saved as Presets. Please click **Presets...** to save or recall a configuration.

7. DISPLAYPORT REFERENCE SOURCE

DP Reference Source function is using one output channel, DisplayPort Source (DP TX). The corresponding vertical tab can be seen on the left edge of the GUI.

The horizontal tabs on the top of the GUI enable the various functions available for the output channel. Some of the tabs are enabled by default, some only when an applicable license is included. DPTX features the following functions.

- Video pattern generator (Pattern Generator)
- Audio generator (Audio Generator)
- Status information and control of the downstream link (Link)
- EDID editor (EDID)
- DPCD monitor (DPCD)
- HDCP status monitor and control (HDCP)
- FEC feature control and status (FEC)
- Sink DUT Testing Tab.

Pattern Generator Tab

E'	r \Audio Generator \I	Link (EDID (ting \				
Video Pattern Ger	nerator			Custom image			
MST Num	ber of streams 🕴 🚆					^	
CTA 1920 x 1080	@ 60 0Hz	~ 8 bp	- v	Color Bars		~	
	@ 00.0112	• 0 000	<u> </u>				attst.
RGB	\sim	\sim		1	* 1	A V	
CTA 1920 x 1080	@ 60.0Hz	~ 8 bp	- v	Color Bars		~	
RGB				1	* 1		- #1 */200
KGD		~		1	• 1	T	
CTA 1920 x 1080	@ 60.0Hz	8 bp	- v	Color Bars		\sim	
RGB	\sim	\sim		1	* 1	Å	Default.bmp
CT1 4000 4000	0.00						Click on image to load
CTA 1920 x 1080	@ 60.0Hz	✓ 8 bp	- ×	Color Bars		~	
RGB				1	* 1	× ·	
Timing values	Timing values						
Custom		0	1	2	3		
	H-Total	2200	2200	2200	2200		
	H-Start	192	192	192	192		
	H-Active	1920	1920	1920	1920		
	H-Sync Width	44	44	44	44		
	V-Total	1125	1125	1125	1125		
	V-Start	41	41	41	41		
	V-Active	1080	1080	1080	1080		DSC Status and Configuration
	V-Sync Width	5	5	5	5		-
	Frame Rate	60.000	60.000	60.000	60.000		Enable DSC
H	Sync Negative polarit	y 🗌					Send PPS
	Sync Negative polarit						
V-	ownerwegauve polarit	7					Pattern Generator Settings
	age Timings						Apply Auto-apply when valid

Note

The video modes that can be used in MST streams are limited by the overall capability of the DisplayPort link and the capability of the connected DisplayPort Sink or Branch device.



Predefined Timings

UCD-400 includes a set of common predefined video timings. Please find a list of the timings with their major details in <u>Appendix C</u> of this document.

Color Mode

RGB color mode with full range quantization levels will be used with all patterns except with *Color Square Pattern*. This pattern allows the user to select RGB, YCbCr 4:4:4, YCbCr 4:2:2 and YCbCr 4:2:0 color modes. When YCbCr is selected, the Colorimetry dropdown box is enabled and allows selection between ITU-709 and ITU-601. Please find a description of the available test patterns in <u>Appendix D</u> of this document.

Color Depth

You can set the color depth used. The available color depths are: 6, 8, 10, 12 and 16 bpc. Color depth 6 bpc is only available with RGB.

Predefined Video Patterns

UCD-400 has a set of predefined patterns and a possibility to user defined custom pattern. You can select the pattern in the provided combo box. By selecting **Disabled** you can have the links activated but no video data transferred.

Please find a description of the available test patterns in Appendix D of this document.

When MST mode is selected, full selection of test patterns is available only in stream 0

Custom Image Patterns

BMP, PNG, JPG and TIFF files can be loaded from the PC to be used as custom images. The bitmaps will be aligned to the top left hand side corner, displayed at the original resolution, no scaling, cropped to the active area.

MST Operation

Multi-streaming can be enabled from MST check box and selecting the number of streams.

Note Please note that MST and DSC features and cannot be used simultaneously

Pattern Generator Settings

In order to avoid sourcing invalid video mode combinations, the new settings need to be validated by the user by clicking **Apply**. Automatic validation will be applied when **Auto-apply when valid** is checked. The situation that parameters have been changed but not applied is indicated by **bold values** of the parameter.

<i>]]]</i> U(CD-400 [1924C3	12] - DisplayPort Sou	irce and Sink				-	
<u>F</u> ile	View Tools	<u>H</u> elp						
	Pattern Genera	tor Audio Generator			P VFEC VSink DUT Testing			
8	Video Pattern G	enerator					Custom image	
Device	MST Nu	umber of streams 1	\$			^	UNIGRAF	
Ĕ	VESA 4096 x	2160 @ 60.0Hz	✓ 10 bpc	~ 1	White Vertical Stripes $$			
RX DP	RGB	\sim	\sim	1	1 🔹 1 🔹			
g			✓ 8 bpc	\sim				
Event Log DP	RGB	~	\sim	1	1 🗘 1		1.00	
entl			∨ 8 bpc	\sim				
ú	RGB	~	\sim	1	1 1 1		Default.bmp	

Note

Please note that the changes in Pattern Generator tab will not be applied unless the user validates them by clicking **Apply** or when **Auto-apply when valid** is checked.

Custom Timing

Custom Timing feature is enabled with UCD Pro for DP Source license.

Timing values			1	1		
Custom		0	1	2	3	
	H-Total	2200	2200	2200	2200	
	H-Start	192	192	192	192	
	H-Active	1920	1920	1920	1920	
	H-Sync Width	44	44	44	44	
	V-Total	1125	1125	1125	1125	
	V-Start	41	41	41	41	
	V-Active	1080	1080	1080	1080	DSC Status and Configuration
	V-Sync Width	5	5	5	5	-
	Frame Rate	60.000	60.000	60.000	60.000	Enable DSC
H-S	ync Negative polarity					Send PPS
V-S	V-Sync Negative polarity Manage Timings					Pattern Generator Settings
Manag						Apply Auto-apply when vali

The timing parameters can be modified by selecting the **Custom** check-box and editing the fields of the matrix. Enable the new parameters by clicking **Apply** button.

Manage Timings

Custom timings can also be created and edited with pop-up *Timing Editor*. Launch the editor by clicking **Manage Timings**.

/// Timing Edi	tor									-		Х
Current timings:												
Show/Type	Name			Timing v	/alues							^
 Fixed 	VESA 512 CTA 5120 VESA 512 VESA 512 CTA 5120 Other 512 VESA 768 VESA 768	20 x 2160 @ 60 20 x 2160 @ 60 0 x 2160 @ 60 20 x 2160 @ 12 20 x 2160 @ 12 0 x 2160 @ 120 20 x 2880 @ 60 80 x 4320 @ 30 80 x 4320 @ 30	.0Hz [R DHz D.0Hz [D.0Hz [.0Hz 0.0Hz [R .0Hz [R	Active (Active (Active (Active (Active (Active (Active (Active (5120 x 2160), To 5120 x 2880), To (7680 x 4320), To (7680 x 4320), To	otal (52 otal (55 otal (52 otal (52 otal (52 otal (55 otal (52 otal (52 otal (77	80, 2222), Sync (3 00, 2222), Sync (3 00, 2250), Sync (8 80, 2287), Sync (3 00, 2287), Sync (3 00, 2287), Sync (3 00, 2250), Sync (3 40, 4381), Sync (3 50, 4381), Sync (3	2, 6) 8, 10) 2, 10) 2, 8) 8, 10) 2, 5) 2, 5) 2, 8)				
Fixed Fixed Clete Selected	VESA 768	0 x 4320 @ 30.1 80 x 4320 @ 60					00, 4400), Sync (1 40, 4443), Sync (3					>
	Horiz	zontal timing	Vertical tim	nina								
1	Total 550	-	2250		Frame rate	(Hz)	120					
A	ctive 512	0	2160		O Pixel Clock (• •	1485				Clear	
9	Start 216		82		Unixel clock (
Sync v			10				Can't modify fixed	l timina.		U	pdate timi	ing
	arity	legative	Negativ	/e		Name	CTA 5120 x 2160			Ac	dd new tin	ning
									X Cancel		🗸 ок	

In order to create a new custom timing based on one of the standard fixed, timings select the fixed timing and change its name and click **Add new timing** to store.

In order to modify an existing custom timing, select it, modify and click Update timing.

The dialog will make a sanity check for the values entered and will warn the user for any combinations that cannot be used.

Customize Timings List

The timings are shown on the pull-down menu by un-checking the **Show** box. The timings will remain in the list and can be brought back to the pull-down menu, when needed.

Sourcing DSC Compressed Patterns

DSC compressed pattern files can be created with a separate tool called *DCS Compressor*. It can be launched from Tools > DSC Compressor.

OSC Compressor						>
File to compress						
Source File:	C:\Te	mp\Your-image.png				
	4096	x 2160, 32bpp				
Sink DSC capabi	ity regis	ters (DPCD range 0x60 -:	> 0x6f,	hex)		
					Up	date
Compression op	tions					
Color space to us	e:	Output resolutions:				
RGB		1920 x 1440 2048 x 1536	^	Compression Ratio:	8bpc -> 6bpp (4.0 to 1)	\sim
Color depth to us	e:	2048 x 1536 2560 x 1440		Horizontal Slices:	1 Slice	~
8 bpc	\sim	2560 x 1080				
Resize mode:		2560 x 1600 2880 x 1440		Vertical Slices:	1 Slice	~
		4096 x 2160				
Tile / Crop	\sim	3840 x 2160				
Parallel compress	ion:	5120 x 2160 5120 x 2880				
	~	7680 x 4320	~	S	tart Compressor(s)	
4 packers						
4 packers	Ť	1000 / 1020	_			

Select the source bitmap file in **Source File** field. Define the **Output Resolution**, the color depth, compression ratio and number of horizontal and vertical slices in the frame.

Click Start Compressor(s).

A DSC compressed file named e.g. *Your_Picture_4096_2160_8.dsc* will be created in the same folder are your source file *Your_Picture*. The selected resolution and bit depth will be added to the file name.

Video Pattern Generator		(Link (EDID (DPCD (H	IDCP (FEC \Sink DUT Testing \	Queters incere		
				Custom image		
	per of streams 1	\$				
CTA 4096 x 2160	@ 60.0Hz	✓ 8 bpc	DSC Image	×		
RGB		\sim	1 1			
		✓ 8 bpc				
RGB	\sim	\sim	1 1			
		\sim 8 bpc \sim				
RGB	\sim	\sim	1 1	Your-image_4096_2160_8.dsc		
		✓ 8 bpc		Click on image to load		
RGB	\sim	\sim	1 1			
Timing values						
Custom		0				
	H-Total	4400				
	H-Start	216				
	H-Active	4096				
	H-Sync Width	88				
	V-Total	2250				
	V-Start	82				
	V-Active	2160				
	V-Sync Width	10		DSC Status and Configuration		
	Frame Rate	60.000		Enable DSC		
H-S	Sync Negative polari	ity 🗌 🗌				
V-5	Sync Negative polari			Send PPS		
				Pattern Generator Settings		
	ige Timings			Pattern Generator Settings		

Select Enable DSC and click Apply.

Note	Please note that the output resolution has to match the size of the used compressed DSC image.
Note	Please note that MST and DSC features and cannot be used simultaneously

Audio Generator Tab

Audio generator allows the user to play LPCM audio generated internally or from files in WAV format.

<u>V</u> iew <u>T</u> ools <u>H</u> elp		
$\label{eq:pattern Generator} \verb Audio Generator \verb Link \verb EDID \verb DPCD \verb HDCP \verb FEC \verb Sink DUT Testing \verb \\$		
Audio Status Audio Ioaded: 2 channels @ 44100 Hz, 16 bits		
Play control		
Audio from: Audio generator. Stopped		
Audio Content		
Generate audio:		
Waveform: Sine V Bits/Sample: 16 bits V		
Signal frequency: 1000 Amplitude: 60%		
Sample Rate: 44100 Hz V Channels: 2 Channels V		
O Load audio from file:		
Open WAV file		

To load internally generated audio, select **Generate audio**, and adjust the controls to the desired audio format.

- To load an audio file from your PC, select **Load audio from file**, click the **Open WAV file...** button, browse and select the file and click **Open**
- ► To play the selected audio content, click the **Play** ► button.

The content will be looped until the **Stop** • button is clicked.

Audio Status in the top of the tab indicates the type of the currently played audio content.

Link Tab

Link tab shows the status and control items for the DisplayPort link.

<u>File Vi</u>	D-400 [1924C312] - DisplayPort Source and Si iew <u>I</u> ools <u>H</u> elp Pattern Generator \/Audio Generator \/Link \/EDID		DUT Testing \			_		×
Devio	HPD Asserted							
Event Log/DP RX/C	600 600 600 600 Cha 0 0 0 0 Pre 0x0000 0x0000 0x0000 0x0000 Errs	ops): 8.1 (HBR3) ode: Enhanced	Link Configuration Number of Lanes 1 2 0 4 Bit rate, Gbps 1.62 2.70 5.40 6.75 8.10 Enhanced Framing Mode Link training Fast Link training Fast Link training Fast Link training Fast Link training Fast Link traini					
	Output Level Voltage Swing, mVpp: 400 600 800 1200 Pre-Emphasis, dB 0 3.5 6.0 9.5 	Link Pattern Active video Idle Pattern Training Pattern 1 Training Pattern 2 Training Pattern 3 Training Pattern 4 PRBS7 HBR2 Compliance EYE SER (Symbol Error Rate)		CRC 0x3F3A Creat Green CRC: 0x967D D Blue CRC: 0xA7BF Cor DSC CRC Value 0: 0x343C Value 1: 0x5D57 Value 2:				

HPD

The status LED indicates the state of the HPD signal Asserted (logical "high") or Deasserted (logical "low").

Link status

The panel shows the result of the link training with the connected downstream sink and status of connection features.

Output Level

Override output level and pre-emphasis values selected during link training. Click **Apply Overrides** to validate changes.

Note Please note that connected Sink and Source actively maintain the link. If the override settings result in link failure, the link will be automatically re-trained and proper values set.

Link configuration

Set target capabilities for the link training. Click **Link Training** to apply.

- Set the Number of Lanes used,
- Set the maximum Link Rate,
- Enable Enhanced Framing Mode

Link Pattern

Select between Active video and audio, Idle pattern or special bit patterns.



CRC

The 16-bit **CRC** (checksum, cyclic redundancy check) values of the three color components calculated by the Sink hardware.

The 16-bit **DSC CRC** values of the captured DSC compressed frame. "Value 0" is calculated from 1^{st} , 4^{th} , 7^{th} ... byte, "Value 1" from 2^{nd} , 5^{th} , 8^{th} ... byte and "Value 2" from 3^{rd} , 6^{th} , 9^{th} ... byte.

EDID Tab

EDID tab enables analyzing and saving the EDID read from the connected Sink device.

1 T.	iew Iools Help Pattern Generator \Link \EDID \DPCD \HDCP \FEC \Sink DUT Testing \			
	Pattern Generator (Audio Generator (Link / EDID (UPCD (HDCP (HEC (Sink DUT Testing)			
	· · · · · · · · · · · · · · · · · · ·		EDID Files	
	000000 00 ff ff ff ff ff ff 00 54 c7 36 40 4c 34 32 30	^		
- 11	000010 34 18 01 04 e5 3d 23 78 3a 5f b1 a2 57 4f a2 28 000020 0f 50 54 bf ef 80 71 4f 81 00 81 c0 81 80 a9 c0		Load	
5	000030 b3 00 95 00 d1 c0 4d d0 00 a0 f0 70 3e 80 30 20		Save as	
	000040 35 00 5f 59 21 00 00 1a 56 5e 00 a0 a0 a0 29 50		56VC 03	
a -	000050 30 20 35 00 5f 59 21 00 00 1a 00 00 00 fd 00 38			
	000060 4b 1e 86 36 00 0a 20 20 20 20 20 20 00 00 00 fc			
	000070 00 55 43 44 2d 34 30 30 20 44 50 31 0a 20 01 de 000080 02 03 12 71 83 4f 00 00 29 0f 7f 07 15 06 55 3d		HEX Editor	
	000090 1f c0 00 00 00 00 00 00 00 00 00 00 00 00		Clear	
- o	0000a0 00 00 00 00 00 00 00 00 00 00 00		Cicui	
	00 00 00 00 00 00 00 00 00 00 00 00 00		Append file	
			FOR 5 h	
	0000f0 00 00 00 00 00 00 00 00 00 00 00		EDID Editor	
			Connected Sink EDID	
			Read	
		~	Write	

There are three basic functions:

- Read the contents of the EDID of the downstream sink over the DisplayPort link.
- Load and save EDID data files in the host PC
- Edit the EDID contents

EDID Files

With **Load...** and **Save as...** a hex EDID file can be read and written from the PC. Please note that the program does not alter the contents of the EDID file or verify its integrity during load and save operation.

Note

Four blocks (512 bytes) of EDID code is read. If the device is not supporting all four blocks, the non-supported area is replaced with zeroes.

Currently the EDID Editor does not support Display ID. Hex EDID files can however be modified with the HEX Editor or externally generated hex EDID files that have Display ID content can be load and programmed into the hardware.

HEX Editor

When EDID content is either loaded from a file or read from the hardware EDID memory, it is shown in the *EDID Data* panel on the left hand side of the dialog. EDID contents can be edited by typing over the existing values. Altered content is highlighted with **RED**. Please note that Hex Editor itself does not alter the contents of the EDID data or verify its integrity.

After editing the data can either be saved to an *.ecd file in the PC with **Save as...** or programmed it to the hardware EDID memory with **Write**.



EDID Editor

EDID Editor is launched in a separate pop-up window. Please see the description of the EDID editor in Chapter <u>EDID Editor</u> later in this document.

DID Editor			-	×
Z EDID Editor E-EDID Encoder / Decoder	Details of ":/0/Version/Vendor_Product Key ID Manufacturer Name ID Product Code ID Serial Number Manufacture or Model year Week of manufacture Year of manufacture	ID* Value UFG 0x4036 0x3032344c Manufacture Year and Week Week 52 Year 2014	-	×
- Sink Underscans IT video - Basic audio - YCbCr (4:4:4) - YCbCr (4:2:2) - Native DTD's in entire E-EDID - 18-8yte Descriptors in this block > CEA Data block count Carton Carton Control Contr	2 Show Log			

DPCD Tab

DPCD tab is a tool for monitoring and editing the DPCD registers of the connected Downstream Sink.

UCD-400 [1924C312] - Dis	playPort Source and Sink				-		Х
le <u>V</u> iew <u>T</u> ools <u>H</u> elp							
/Pattern Generator Audi	lio Generator (Link (EDID) DPC	HDCP FEC Sink DU	T Testing				
DPCD Decoder 1.4 + DET	TAILED_CAP_INFO_AVAIL = 0	~		🔁 Load		🔛 Save	
DPCD Decoder 1.4 + DET DPCD Address range: 0x0	Number of bytes to	read: 0x 100					
A 0000001 14 1<	$\begin{array}{c} 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	↓ √ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	Link/Sink Device Status SINK_COUNT [RO] 0x00200 := 0x41 SINK_COUNT = 1 CP_READY = 1			~
			7 White Changes	-			
DPCD Address range: 0x 2	200 Number of bytes to	read: 0x 100					
000210 00 80 00 8 000220 00 00 00 0	7 01 03 11 11 00 00 00 0 00 80 00 80 00 00 00 0 00 00 00 00 00 00 00 00 0 00 0	00 00 00 00 00 00 00 00 00 00	^				
000240 3a 3f 7d 9 000250 00 00 00 0	6 bf a7 27 00 00 00 00 00 0 00 00 00 00 00 00 00 0	00 00 00 00 00 00 00 00 00 00					
000270 00 00 00 0	0 00 00 00 00 00 00 00 00 00 00 00 00 0	00 00 00 00 00	~				
Set Reference		🚯 Refresh	😴 Write Changes				
				L			-

The tool consists of two independent monitoring and editing windows for the DPCD data. The user can freely select the the DPCD address areas shown on each panel.

The *DPCD Decoder* panel on the right hand side shows the interpretation of the DPCD byte selected on the monitoring windows. The selected byte is shown with a green outline.

In the combo box above the DPCD Decoder window you can select how the DPCD data is interpreted, either as *DP 1.1 DPCD*, or as *DP 1.2 DPCD* with *Detailed Capability Info* selected or not (DETAILED_CAP_INFO_AVAIL = 1/0).

By clicking **Refresh** you can re-read the data from the DPCD registers to the window in question.

By clicking **Write Changes** you can write the portion of data shown in the window in question to the DPCD registers.

By clicking **Set Reference** you can store currently shown data as a reference for comparison.

When you refresh the data from the DPCD registers the changed bytes will be highlighted with gray background.

The fields edited by the user will be highligted with **red** color.

Saving and Loading DPCD Content

DPCD data in the selected address areas can be saved as a file in your PC. There are three alternative formats:

- Binary *DPCD Fata File* format (*.DPD). This is Unigraf proprietary format. You can also load the DPCD content stored in this format.
- *Comma Separated Values* (*.CSV) for loading the data to a spreadsheet.
- *HEX Dump* (*.HEX) in a human readable text format.
- Click **Save** to select the location and the format of the file.
- Click **Load** to load DPCD data saved in *DPCD Data File* (*.DPD) format to the editor.
- To program the data into the DPCD registers of UCD-400 Local Sink click Write Changes.

Note	- Writing DPCD data to the DPCD registers of the Sink will potentially affect the status and capabilities of sink as seen by the source.
	- User control like Link Training or mode changes will modify the content of the DPCD registers

HDCP Tab

HDCP tab is the dialog for monitoring the HDCP (for *High-Bandwith Digital Content Protection*) status and controlling the HDCP capabilities of the connected UCD-400 device.

		312] - DisplayPort Source and Sir	ık	-	×
<u>F</u> ile	<u>V</u> iew <u>T</u> ools	<u>H</u> elp			
	/Pattern Gener	ator \langle Audio Generator \langle Link \langle EDID	DPCD HDCP FEC Sink DUT Testing		
Event Log DP RX DP TX Device	HDCP 1.3 Status		Configuration Enable encryption Authenticate Keys Production		
ent Lo			○ Facsimile - "Test" ○ None		
L.			Churc		
	HDCP 2.3				
	Status		Configuration		
		Active Authenticated Authentication in progress Keys loaded	Authenticate		

Status

The status fields indicate the HDCP status of the connected UCD-400 device.

Active: The stream between UCD-400 and the downstream sink has been encrypted.

Authenticated: The HDCP handshake between the UCD-400 and the sink unit has been completed successfully.

Authentication in process: The HDCP handshake is in process between the UCD-400 and the downstream sink unit.

Keys loaded: The HDCP keys are loaded to the UCD-400 unit.

Configuration

Enable encryption: Check to enable the encryption of the stream between UCD-400 and the downstream sink.

Authenticate: Perform the HDCP initiation handshake between the UCD-400 and the sink unit.

Keys

Select between Production or Facsimile HDCP keys. To remove the keys, select None.

HDCP 1.3 vs. HDCP 2.3

UCD-400 devices support by default HDCP 1.3 and HDCP 2.3.

FEC Tab

Forward Error Correction (FEC) can be enabled if connected sink supports it. For debug purposes, error injection to main-link is possible. There is an error type for each standard sink DPCD error counter.

	FEC Enabled	Prefer FEC E	nabled		Enable FEC	Disable FEC	
En	rror generator					FEC Status Log	
N	Number of errors to general	te for Lane #0:		0		Sink FEC Status: Decode Disable Detects Sink FEC Status: Decode Enable Detecte	NOT detecte
N	Number of errors to general	te for Lane #1:		0	÷	Sink i EC Status, Decode Enable Detecte	
	Number of errors to general			0			
	-			-			
N	Number of errors to general	te for Lane #3:		0	•		
0	Generate errors of type:		Corre	cted parity 1	error 🗸 🗸		
C	Delay between steps (in milli	iseconds):		0			
				-			
				58 Ap	ply		
Sin	nk Error Counters (DPCD)						
		Lane #0	Lane #1	Lane #2	Lane #3		
	Incorrected block errors	0	0	0	0		
_	Corrected block errors	0	0	0	0		
	Bit errors	0	0	0	0		
	arity block errors	0	0	0	0		
Pa	arity bit errors	0	0	0	0		
		Vpdate		💋 Clear co	unters		
		opulate		p cica co	Jantero		
De	ebug FEC Sequencing						
	Send FEC Enable Seq			FEC Disable !	-		

FEC

Clicking **Enable FEC** UCD-400 will verify if connected sink supports FEC and begins the handshake for enabling FEC.

Clicking **Disable FEC** UCD-400 will start the FEC disable handshake.

If **Prefer FEC Enabled** is selected and the connected sink supports FEC, UCD-400 will start the FEC Enable Sequence after a successful connection.

Error Generator

Generate errors of type: selection will set how many errors will be inserted into one FEC block and to which link symbols. There are five options:

- Uncorrected block: 3 symbol errors with 3 error bits together
- Corrected block: 2 symbol errors with 2 error bits together
- Corrected parity: 2 parity byte errors with 2 error bits together
- Corrected block 1 error
- Corrected parity 1 error

Note: FEC must be enabled and running before errors can be added.



Each lane can have its individual error amount. Errors can be injected to even and odd decoders by using **lane #0** and **lane #1** counters when link is configured to one lane.

Clicking Apply will start error injection.

Clicking Update will read sink DPCD FEC error counter registers.

Clicking Clear counters will clear sink DPCD FEC error counter registers.

Note: Link training will reset sink FEC error counters.

Debug FEC Sequencing

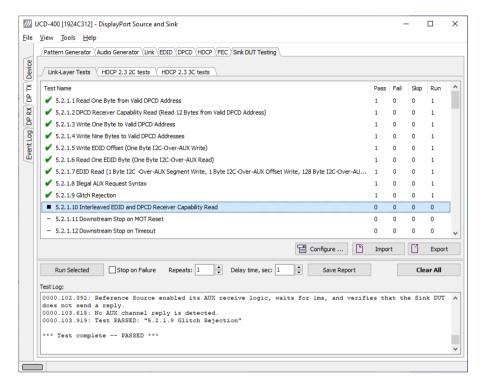
When clicking **Send FEC Enable Sequence** UCD-400 will start adding *FEC Enable Sequence* in its main link data.

When clicking **Send FEC Disable Sequence**, UCD-400 will start adding *FEC Disable Sequence* in its main link data.

Sink DUT Testing Tab

Sink DUT Testing Tab is enabled with UCD Pro for DP Source license.

Please refer to **Appendix E** later in this document for description of the tests available. Sink DUT Testing enables the execution of HDCP 2.3 Compliance Tests for a DP Sink DUT. Sink DUT Testing enables testing of a DP Sink DUT. Please refer to **Appendix E** of this document to get a full definition of the Test Cases and test parameters.



Select the tests for execution by clicking the corresponding row.

Clicking **Configure...** opens a dialog for defining the test parameters for that set. Please refer to *Test Parameters* below for description.

Parameters from *Test descriptor files* can be loaded with **Import** and stored with **Export**. Please refer to documentation of TSI software API for description.

Tests are started by clicking **Run Selected**. By clicking **Abort** the sequence is stopped.

Test flow can be controlled with **Repeats** of the test sequence, **Delay** between individual tests or **Stop on Failure** that stops the whole sequence if one of the tests fail.

At the completion of each test the result of the test is indicated in the matrix on the right hand side of the test panel. For each test the matrix lists the number of occurrences of each result and the number of tries performed.

Click **Save Report** to generate a HTML report file for sharing the results with other parties for viewing without UCD Console.

By clicking Clear All the test log and the results matrix are cleared.

Test Parameters

Each test set has its dedicated set of test parameters. To open a dialog for defining the parameters click **Configure...**

Parameters of LL CTS Tests

Link-Layer Tests parameter panel defines which resolutions and video modes are used for testing.

DP 1.4 LL CTS DUT Sink Capabilities		_		×
Test Parameters				
Test timeout, milliseconds:	1000000			
Use video mode(s) from:	Use test configuration (below	v)	\sim	
	CTA RB1 RB2			
1920 x 1080 @ 30 Hz:				
1920 x 1080 @ 60 Hz:				
1920 x 1080 @ 120 Hz:				
3840 x 2160 @ 30 Hz:				
3840 x 2160 @ 60 Hz:				
3840 x 2160 @ 120 Hz:				
5120 x 2160 @ 30 Hz:				
5120 x 2160 @ 60 Hz:				
5120 x 2160 @ 120 Hz:				
7680 x 4320 @ 30 Hz:				
7680 x 4320 @ 60 Hz:				
7680 x 4320 @ 100 Hz:				
	Set / Clear All			
Presets	🗸 ок	×	Cancel	

They can be defined in the matrix in the dialog by selecting **Use test configuration (below)** or determined by evaluating content of DUT EDID by selecting **Use sink DUT EDID**.

Parameters of HDCP CTS Tests

HDCP CTS Tests have their own parameter dialog.

DP HDCP CTS 3C test parameters -							
Test Parameters							
Test timeout, milliseconds	200000						
Repeater_MultipleOutputs	1						
Number of Sinks connected to Repeater	0						
Cancel							

Saving and Loading Presets

In all parameter dialogs the selected parameters can be saved as Presets. Please click **Presets...** to save or recall a configuration.

8. COMPLIANCE TESTS

Compliance test capability is a license enabled add-on to UCD Console.

The tests are included in the GUI software, license codes enable the tests for use. Please refer to *Appendix B Licensing* for details. The list of compliance tests that UCD Console supports, please refer to document *DP CTS Tool Options for Unigraf UCD-400.pdf*. It can be downloaded in Unigraf Document Center at

<u>www.unigraf.fi/support/downloads/documents.</u> If you have any additional questions, please contact Unigraf or your local representative.

Compliance tests (CTS Tests) are part of tests included in **Source DUT Testing** tab of **DP RX** and **Sink DUT Testing** tab of **DP TX**.

UCD-400 [1924C312] - DisplayPort Source and Sink			-	-		×	
<u>File View T</u> ools <u>H</u> elp							
/Video \{Audio \{Link \{EDID \\DPCD \\HDCP \\SDP \\FEC \\Source DUT Testing \}							
Unk-Layer Tests V HDCP 2.3 1A tests V HDCP 2.3 1B tests V HDCP 2.3 3A tests V HDCP 2.3 3B tests	CRC tests	(Simp	le LT te	ests			
Test Name		Pass	Fail	Skip	Run	^	
- 4.2.1.1 Source DUT Retry on No-Reply During AUX Read after HPD Plug Event		0	0	0	0		
🖉 – 4.2.1.2 Source Retry on Invalid Reply During AUX Read after HPD Plug Event		0	0	0	0		
- 4.2.1.3 Source Device HPD Event Pulse Length Test		0	0	0	0		
- 4.2.1.4 Source Device IRQ_HPD Pulse Length Test		0	0	0	0		
- 4.2.1.4 Source Device IRQ_HPD Pulse Length Test - 4.2.1.5 Source Device Inactive HPD / Inactive AUX Test - 4.2.2.1 DPCN Device receiver Canability and EDIN Device HPD Plus Event		0	0	0	0		
- 4.2.2.1 DPCD Receiver Capability and EDID Read upon HPD Plug Event		0	0	0	0		
- 4.2.2.2 DPCD Receiver Capability Read upon HPD Plug Event 0 0 0 0							
- 4.2.2.3 EDID Read 0 0 0 0							
- 4.2.2.4 EDID Read Failure #1: I2C-Over-AUX NACK 0 0 0 0							
- 4.2.2.5 EDID Read Failure #2: I2C-Over-AUX DEFER 0 0 0 0							
- 4.2.2.6 EDID Corruption Detection 0 0 0 0							
 4.2.2.7 Branch Device Detection upon HPD Plug Event 		0	0	0	0	~	
뎥 Configu	.re 🖺	Impo	rt	[]	Export	t	
Run Selected Stop on Failure Repeats: 1 🗘 Delay time, sec: 1 💌 Sa	ave Report]		Cle	ar All		
Test Log:							
						~	
						\sim	

The tests cases are divided to test categories as described in *Appendix E* of this document. Each test category can be found in its dedicated sub-tab. The sub-tabs as in turn enabled by the licenses present in user's PC. Please refer to chapter 3 *License Manager* earlier in this document.

DSC Test Content

When running DSC Compliance Tests, UCD-400 needs to have access to DSC content used as test patterns. The content can be created from the source bitmap files downloaded during installation (optional) either with Unigraf DSC Content Creator or created by the Compliance Test Tool on-the-fly during the compliance test.

Options

In Tools > Options menu you can define DSC Work folder DSC test content directory.

You can also select to *Automatically create missing content*, automatically create the DSC compressed content used for testing the DUT. You can also *Keep auto-created DSC content files:* By default, the DSC compressed content is deleted after use. If selected, the content is not kept, not deleted.

Warning Keeping the automatically created DSC compressed content will shorten the time needed for running the DSC compliance tests.

Please note, that the space needed for storing the full library **can be very large** (appr. 100 GBytes). Please make sure that the content will be stored in a medium that has the required space available.

Test Parameters

Before running the tests, capabilities of the DUT has to be defined for the test engine. Each test category has its dedicated test parameter dialog. Click **Configure...** in *Source DUT Testing* or *Sink DUT Testing* tab to open the parameter dialog.

0P 1.4 LL CTS DUT Source Capabilities									
General Audio DSC									
Test timeouts		Colorimet	бу						
Test timeout (milliseconds):	5000	* *	RGB		YCbCr 4:2:2		YCbCr 4:4:4		
Long HPD pulse duration (milliseconds):	1000	🛉 🗹 6bpc \	/ESA	🗌 8b	pc CTA (ITU.601)		8bpc CTA (ITU.601)		
LT Start timeout (milliseconds):	5000	8bpc	/ESA	10	bpc CTA (ITU.601)] 10bpc CTA (ITU.601)		
Test cycle delay (milliseconds):	5000	10bpc	VESA	🗌 8b	pc CTA (ITU. 709)		8bpc CTA (ITU. 709)		
DUT Capabilities	5555	Bbpc (CTA	10	bpc CTA (ITU. 709)] 10bpc CTA (ITU. 709)		
Max lanes supported:	4 Lanes	10bpc	CTA						
Max bit rate supported:	HBR3 (8.10 Gbps)	Select	All						
Voltage Swing level 3 (1.2V) supported		Video Mo	des						
Pre-Emphasis level 3 (9.5dB) supported	1	Tell and a			640x480 @ 60Hz 6 I	200			
Fixed timing DUT									
Spread Spectrum Supported		Maximum	Maximum supported video mode: 3840x2160 @ 60Hz 8 BPC					\sim	
Video format change without LT suppor	ted	Most Pad	ked Timings						
Lane count reduction without LT support	rted		-						
E-DDC supported			1 Lane 1280 x 800 @ 60Hz 6bpc					~	
Audio Info Frame supported for 2 chan	nel audio	2 Lanes	2 Lanes 1280 x 1024 @ 60Hz 8bpc					\sim	
DUT is Type-C Device		4 Lanes	Lanes 2048 x 1536 @ 60Hz 8bpc					\sim	
FEC supported		Time-star	np generation						
FEC disable sequence supported		Time orde	1 Lane		2 Lanes		4 Lanes		
Audio without Video supported		RBR	848x480@60 Hz	~	1280x720@60 Hz	~	1920x1080@60 Hz	\sim	
Test Automation TEST LINK TRAINING		HBR	1280x720@60 Hz	~ ~	1280x960@60 Hz	~	1920×1080@60 Hz	~	
TEST EDID READ					-		-	•	
		HBR2	1280x960@60 Hz		1920x1080@60 Hz	~	1920x1080@120 Hz	~	
TEST_AUDIO_PATTERN		HBR3	1792x1344@60H	z v	3840x2160@30Hz	\sim	3840x2160@60Hz	\sim	
Event indicating DUT ready:	Active Video	\sim							
Presets					🗸 (Ж	X Cance	el	

For a detailed description of capabilities listed on the tab please refer to *Chapter 3 Compliance Test Operation* of document *VESA DisplayPort v1.4a Link Layer Compliance Test Specification*.

Note Please make sure that the capability tables are completed before running the tests. The result of the test might be misleading if the DUT capabilities and the table do not match.

Saving Test Parameters

Test parameters can be saved for later use in two ways: internally or externally in a file.

In parameter dialog the parameter set can be saved as an internal Preset.

In *Source* or *Sink DUT Testing* tab **Export** saves test definitions of each selected test in a separate file. **Import** loads the parameters back to UCD Console. They can be run with Unigraf TSI. Please refer to chapter 7.3.6 *Running Tests* in document *TSI-X_Reference.pdf* in UCD Console release package.

Running CTS Tests

Source DUT Testing and *Sink DUT Testing* tabs include the tests enabled with the set of licenses present in UCD Console. The tests are grouped in test set tabs. In tabs the tests are listed by the test name and reference number as presented in applicable compliance test specification. UCD-400 firmware implements the test according to the test specification.

For running a test, select it and click **Run selected**. For selecting multiple consecutive tests in the list hold down the **Shift** key of your keyboard while selecting the tests. For selecting multiple individual tests hold down the **Ctrl** key in your keyboard while selecting.

File Yiew Jools Help Video (Audio (Link (EDID (DPCD (HDCP (SDP (FEC) Source DUT Testing) Unk-Layer Tests (HDCP 2.3 1A tests) (HDCP 2.3 3A tests) (HDCP 2.3 3B tests) CRC tests) Simple LT tests Test Name Pass Fail Skip Nu 0 0 0 0 4.2.1.1 Source DUT Retry on No-Reply During AUX Read after HPD Plug Event 0	UCD-400 [1924C312] - DisplayPort Source and Sink		-	-		\times
Unk-Layer Tests HDCP 2.3 1A tests HDCP 2.3 3B tests HDCP 2.3 3B tests CRC tests Simple LT tests Test Name Pass Fail Skip Run 4.2.1.1 Source DUT Retry on No-Reply During AUX Read after HPD Plug Event 0 0 0 0 4.2.1.2 Source Device Retry on Invalid Reply During AUX Read after HPD Plug Event 0 0 0 0 0 4.2.1.3 Source Device IRQ_HPD Pulse Length Test 0 0 0 0 0 0 4.2.1.4 Source Device IRQ_HPD Pulse Length Test 0	<u>File View T</u> ools <u>H</u> elp					
Image: Configure	Video (Audio (Link (EDID (DPCD (HDCP (SDP (FEC)) Source DUT Testing)					
Image: Configure	Unk-Layer Tests V HDCP 2.3 1A tests V HDCP 2.3 1B tests V HDCP 2.3 3A tests V HDCP 2.3 3B tests V CRC tests	Simp	le LT te	ests		
Image: Configure		Deer	c.d	Chie	Dura	•
Image: Configure						
• 4.2.1.3 Source Device HPD Event Pulse Length Test 0 0 0 0 • 4.2.1.4 Source Device IRQ_HPD Pulse Length Test 0 0 0 0 • 4.2.1.5 Source Device IRQ_HPD Pulse Length Test 0 0 0 0 • 4.2.1.5 Source Device Inactive HPD / Inactive AUX Test 0 0 0 0 • 4.2.1.1 Source Device Inactive HPD / Inactive AUX Test 0 0 0 0 • 4.2.2.1 DPCD Receiver Capability and EDID Read upon HPD Plug Event 0 0 0 0 • 4.2.2.2 DPCD Receiver Capability Read upon HPD Plug Event 0 0 0 0 • 4.2.2.3 EDID Read 0 0 0 0 0 • 4.2.2.4 EDID Read Failure #1: 12C-Over-AUX NACK 0 0 0 0 • 4.2.2.5 EDID Read Failure #1: 12C-Over-AUX DEFER 0 0 0 0 0 • 4.2.2.6 EDID Corruption Detection 0 0 0 0 0 v • 4.2.2.7 Branch Device Detection upon HPD Plug Event 0 0 0 v v • Configure • Import • Export • Export <						
Image: Configure Config		-	-	-	-	
- 4.2.2.2 DPCD Receiver Capability Read upon HPD Plug Event 0 0 0 0 0 - 4.2.2.3 EDID Read 0 0 0 0 0 0 - 4.2.2.3 EDID Read Failure #1: I2C-Over-AUX NACK 0 0 0 0 0 - 4.2.2.5 EDID Read Failure #2: I2C-Over-AUX DEFER 0 0 0 0 0 - 4.2.2.6 EDID Corruption Detection 0 0 0 0 0 0 - 4.2.2.7 Branch Device Detection upon HPD Plug Event 0 0 0 0 0 v Import Import Import Import Export			-			-
- 4.2.2.2 DPCD Receiver Capability Read upon HPD Plug Event 0 0 0 0 0 - 4.2.2.3 EDID Read 0 0 0 0 0 0 - 4.2.2.3 EDID Read Failure #1: I2C-Over-AUX NACK 0 0 0 0 0 - 4.2.2.5 EDID Read Failure #2: I2C-Over-AUX DEFER 0 0 0 0 0 - 4.2.2.6 EDID Corruption Detection 0 0 0 0 0 0 - 4.2.2.7 Branch Device Detection upon HPD Plug Event 0 0 0 0 0 v Import Import Import Import Export		-	-	-	-	J
- 4.2.2.2 DPCD Receiver Capability Read upon HPD Plug Event 0 0 0 0 0 - 4.2.2.3 EDID Read 0 0 0 0 0 0 - 4.2.2.3 EDID Read Failure #1: I2C-Over-AUX NACK 0 0 0 0 0 - 4.2.2.5 EDID Read Failure #2: I2C-Over-AUX DEFER 0 0 0 0 0 - 4.2.2.6 EDID Corruption Detection 0 0 0 0 0 0 - 4.2.2.7 Branch Device Detection upon HPD Plug Event 0 0 0 0 0 v Import Import Import Import Export	4.2.1.5 Source Device Inactive HPD / Inactive Aux Test				-	
- 4.2.2.3 EDID Read 0 0 0 0 0 - 4.2.2.4 EDID Read Failure #1: 12C-Over-AUX NACK 0 0 0 0 0 - 4.2.2.5 EDID Read Failure #2: 12C-Over-AUX DEFER 0 0 0 0 0 - 4.2.2.6 EDID Corruption Detection 0 0 0 0 0 0 - 4.2.2.7 Branch Device Detection upon HPD Plug Event 0 0 0 0 v Import Import Import Export	1.2.2.1 Dr Co Receiver Capability and EDD Read aport in D hig Event	-	-	-	-	
- 4.2.2.4 EDID Read Failure #1: 12C-Over-AUX NACK 0 0 0 0 0 - 4.2.2.5 EDID Read Failure #2: 12C-Over-AUX DEFER 0 0 0 0 0 - 4.2.2.6 EDID Corruption Detection 0 0 0 0 0 0 - 4.2.2.7 Branch Device Detection upon HPD Plug Event 0 0 0 0 0 √ Configure		-		-		
- 4.2.2.5 EDID Read Failure #2: 12C-Over-AUX DEFER 0 0 0 0 0 - 4.2.2.5 EDID Corruption Detection 0 0 0 0 0 0 - 4.2.2.7 Branch Device Detection upon HPD Plug Event 0 0 0 0 0 0 v Import Import Import Import Import Import Import Import		-	-	-	-	
- 4.2.2.6 EDID Corruption Detection 0		-	-	-	-	
- 4.2.2.7 Branch Device Detection upon HPD Plug Event 0 0 0 0 0 v Import Import Import Import Import Export Run Selected Stop on Failure Repeats: 1 Delay time, sec: 1 Save Report Clear All		-		-	-	
Import Import Run Selected Stop on Failure Repeats: 1 Delay time, sec: 1 Save Report Clear All		-	-	-	-	
Run Selected Stop on Failure Repeats: 1 • Delay time, sec: 1 • Save Report Clear All						~
	E Configure	Impor	rt	Ľ	Export	:
Test Log:	Run Selected Stop on Failure Repeats: 1 Delay time, sec: 1 Save Report]		Cle	ar All	
	Test Log:					
						^
· · · · · · · · · · · · · · · · · · ·						~

Repeats defines number of test-runs and the **Delay time** delay between the tests. When repeating a sequence of tests, all selected tests are performed in each repetition. E.g. when you repeat tests 1, 2 and 3 two times, the sequence is: 1, 2, 3, 1, 2, 3.

Test flow parameters like **Test timeout** and **Test cycle delay** can be defined in *Test Parameter* dialog launched by clicking **Configure...**

Selecting Stop on Failure stops execution of a series of tests in case a failure is found.

For clearing the Status Log and the Results matrix, click Clear All.

Evaluating CTS Test Results

The test procedure advancement can be monitored in the *Test Log* panel. It describes the steps of each individual test in the way defined in the corresponding VESA Compliance Test Specification. Please use the Status Log and Specification side by side when interpreting the results.

At the completion of each test the result of the test is indicated in the matrix on the right hand side of the test panel. For each test the matrix lists the number of occurrences of each result and the number of tries performed.

UCD-400 [1924C312] - DisplayPort Source and Sink		-		×				
<u>File View Tools H</u> elp								
/Video \Audio \Link \EDID \DPCD \HDCP \SDP \FEC \Source DUT Testing \								
Unk-Layer Tests / HDCP 2.3 1A tests / HDCP 2.3 1B tests / HDCP 2.3 3A tests / HDCP 2.3 3B tests / CRC test			_					
/ Link-Layer Tests / HDCP 2.3 1A tests / HDCP 2.3 1B tests / HDCP 2.3 3A tests / HDCP 2.3 3B tests / CRC test	ts 👋 Simple L	T tests	1					
Test Name	Pass	Fail	Skip	Run				
▲ IA-01 Regular Procedure - With previously connected Receiver (With stored km)	1	0	0	1				
Image: State	1	0	0	1				
△ IA-03 Regular Procedure - Receiver disconnect after AKE_Init	1	0	0	1				
S 1A-04 Regular Procedure - Receiver disconnect after km	1	0	0	1				
IA-04 Regular Procedure - Receiver disconnect after km IA-05 Regular Procedure - Receiver disconnect after locality check IA-05 Regular Drocedure - Receiver disconnect after locality check	0	0	0	0				
A-06 Regular Procedure - Receiver disconnect after ks	0	0	0	0				
 1A-07 Regular Procedure - Receiver sends REAUTH_REQ after Ks 	0	0	0	0				
- 1A-08 Irregular Procedure - Verify Receiver Certificate	0	0	0	0				
- 1A-09 Irregular Procedure - SRM	- 1A-09 Irregular Procedure - SRM 0 0 0 0							
- 1A-10 Irregular Procedure - Invalid H'	0	0	0	0				
- 1A-11 Irregular Procedure - Pairing Failure	- 1A-11 Irregular Procedure - Pairing Failure 0 0 0 0							
 1A-12 Irregular Procedure - Locality Failure 	0	0	0	0				
E Configure	j Import	Ľ] E	kport				
Run Selected Stop on Failure Repeats: 1 😴 Delay time, sec: 1 😴 Save Report			Clear	All				
Test Log:								
0002.454.648: [TE-Snk] STEP 1A-04-1 0002.553.641: [TE-Snk] WARNING. DUT sends unencrypted video 0002.553.675: [TE-Snk] DUT initiates authentication by transmitting AKE_Init 0002.554.081: Test PASSED: "1A-04 Regular Procedure - Receiver disconnect after km"				^				
*** Test complete PASSED ***				*				

Test Report

Results of the test can be saved as a report in HTML format.

Click **Save Report** in UCD Console. A dialog will open where information about the DUT and remarks about the test can be included in the report. Details of the used test equipment and the software and firmware version will be added automatically.

/// Report information	- 🗆 ×
UCD-400 [1924C312]	DUT Information
Serial number:	Model:
1924C312	ABC
Firmware package:	Serial Number:
MN 1.8.11 MF 1.7.9	1234567890
Application Version	Revision:
Version 1.9 [R0], Build# 25582	Firmware version:
	Driver:
Report Information	
Tested by: Tester	
Remarks: (1024 chars max.)	
L	
	🗸 Save 🔀 Cancel

Viewing the CTS Test Report

The report file can be viewed with any HTML browser. The report has built-in views for Report Summary, Test Summary and individual Test Logs.

Unigraf Test Report	× +		-		
)→ C û	Q, file:///C:/Users/aaa/Desktop/test.html	± 1	I\ 🗉	۲	
Total number of test runs: 4 Passed test runs: 4 Failed test runs: 0 Skipped test runs: 0 Aborted test runs: 0					
EST DETAILS, TEST 1					
1A-01 Regular Procedu	e - With previously connected Receiver (With stored km)				
Test Result: PASSED					
Test Settings: Test timeout, milliseconds : Revoke ID = 71.6A.15.46 B Source_EncDisableBootst	F				
Test Log					
0000.000.146: [TZ=-3: 0000.000.256: [TZ=-3: 0001.001.163: [TZ=-3: 0001.001.163: [TZ=-3: 0001.001.163: [TZ=-3: 0001.001.290: [TZ=-3: 0001.100.021: [TZ=-3: 0001.100.021: [TZ=-3: 0001.255.917: [TZ=-3: 0001.255.917: [TZ=-3: 0002.232.047: [TZ=-3: 0002.232.047: [TZ=-3: 0002.232.047: [TZ=-3: 0002.232.147: [TZ=-3: 0002.242.664: [TZ=-3: 0002.242.664: [TZ=-3: 0002.243.080: [TZ=-3: 0002.243.080: [TZ=-3: 0002.243.080: [TZ=-3: 0002.243.080: [TZ=-3: 0002.244.090: [TZ=-3: 0002.244.090: [TZ=-3: 0002.244.090: [TZ=-3: 0002.244.090: [TZ=-3: 0002.244.090: [TZ=-3: 0002.244.090: [TZ=-3: 0002.244.090: [TZ=-3: 0002.244.852: [TZ=-3: 0002.254.852: [TZ=-3: 0002.554.952: [TZ=-3:	 XE transmits Receiver Connected Indication(Hot plug, CONNECTION_STATUS_NOTIFY and k] [Authentication and Key Exchange] STEP 1A-01-2 MARING. DUT sends unencrypted video MARING. DUT sends unencrypted video STEP 1A-01-3 MARING. DUT sends unencrypted video DUT initiates authentication by transmitting AKE_Init STEP 1A-01-3 AKE_Send_Cert message is available DUT sends AKE_No Stored_Lm message Send AKE_Send_Firing_Info message Send AKE_Send_Firing_Info message Store 1A-01-4 STEP 1A-01-4 DUT sends LC_Bend_L prime message STEP 1A-01-4 DUT sends LC_Bend_L prime message STEP 1A-01-4 DUT sends LC_Bend_L prime message STEP 1A-01-4 DUT sends SKE Send_Els message STEP 1A-01-6 DUT sends SKE Send_Els message STEP 1A-01-6 STEP 1A-01-6 STEP 1A-01-7 Checking the correctness of the LINK_VERIFICATION_PATTERN within the first 48VB-ID Authentication and link integrity check complete ANSED: "1A-01 Regular Procedure - With previously connected Receiver (With stored km)" 	_		ion	
EST DETAILS, TEST 2					
1A-02 Regular Procedu	re - With newly connected Receiver (Without stored km)				
Test Result: PASSED					

9. EVENT LOG

Event Logger (Event Log) vertical tab can be seen on the left edge of the GUI. Event Log is enabled with UCD Pro for DP Sink or UCD Pro for DP Source license.

Event Log dialog is divided into two panels: the left panel lists all transactions and the right panel shows the parsed transaction data for the line selected in the list on the left.

e I r	<u>V</u> iew <u>T</u> ools <u>H</u> elp								
	Start Capture	III S	top Capt	ure					
	Data sources and filters:		/Event	Log VDP AUX anal	vzer (DP Ou	tout port)	OP AUX analyzer (DP Input port)		
	✓ · DisplayPort Output		Г <u> </u>		Report				
	🕅 HPD			Jave	Report		pen		
	AUX		#	Timestamp	Type	From F	Data /	•	
	 DisplayPort Input 		1	1561854.924	HPD	7	HPD High, Cable Connected, Power pres.		
21			2	1574733.015	HPD	6	HDP Low, Cable Connected, Power pres.		
	SDP		3	1574786.205	VB	0	09 00 08 00		
	MSA changes		4	1575234.279	HPD	7	HPD High, Cable Connected, Power pres.		
	VB-ID changes		5	1575267.879	AUX	0	90 00 0E 00		
١l	- V Link		6	1575267.991	AUX	8	00 80		
	VB-ID		7	1575268.057	AUX	0	90 22 00 00		
			8	1575268.165	AUX	8	00 14		
Ш			9	1575268.231	AUX	0	9F 00 00 04		
		<	10	1575268.344	AUX	8	00 00 00 00 00 00		
Ш			11	1575268.449	AUX	0	40 00 50 00 00		
Ш			12	1575268.540	AUX	8	00		
Ш			13	1575268.600	AUX	0	50 00 50 0F		
Ш			14	1575268.686	AUX	8	00 00 FF FF FF FF FF FF 00 54 C7 36 40.		
Ш			15	1575268.880	AUX	0	50 00 50 0F		
Ш			16	1575268.966	AUX	8	00 34 18 01 04 E5 3D 23 78 3A 5F B1 A2.		
			17	1575269.159	AUX	0	50 00 50 0F		
Ш			18	1575269.245	AUX	8	00 0F 50 54 BF EF 80 71 4F 81 00 81 CO.		
11			19	1575269.438	AUX	0	50 00 50 0F		
11			20	1575269.524	AUX	8	00 B3 00 95 00 D1 C0 4D D0 00 A0 F0 7		
11			21	1575269.717	AUX	0	50 00 50 0F		
			22	1575269.802	AUX	8	00 35 00 5F 59 21 00 00 1A 56 5E 00 A0.		
11			23	1575269.996	AUX	0	50 00 50 0F		
Ш	- .	1	74 <	1575270 081	ΔΗΥ	8	00 30 20 35 00 5E 59 21 00 00 14 00 00		
Ш	Presets								_

With the Event Logger captures the following items

- HPD status (DP TX and DP RX)
- AUX transaction (DP TX and DP RX)
- DP SDP messages (DP RX)
- Changes in MSA (DP RX)
- Changes in VB-ID (DP RX)

Each item line includes Time stamp, Type indication, Message source, and raw message data. The right panel lists the content of one message. Messages belonging together with the selected one are shown in red color.

- Start event logging by clicking Start Capture and stop it by clicking Stop Capture.
- The transactions can be saved in binary *.evt Event Log files by clicking **Save**. Saved Event Log files can be recalled by clicking **Open**.
- Clicking **Report** stores event logs as html reports to be shared and viewed with any web browser. The save dialog allows inclusion of detailed information about the DUT and the test in free-text *Report information*.

DP AUX Analyzer

	Start Capture	I S	top Capt	ure							
2	Data sources and filters:		/Event		analyzer (DP	Output por	t) DP AUX a	nalyzer (DP	Input port) (
5	OisplayPort Output HPD			<u>S</u> ave	Report		Open				
	AUX		Line	Timestamp	From	Туре	Details		Data	1	Message details:
			172 173 174 175 176 177 178 179	1575443.74 1575443.94 1575444.05 1575444.25 1575444.37 1575444.56 1575444.68 1575444.68	Source Sink Source Sink Source Sink HDCP 2.3	Native Native Native Native Native Native Native Trace	Reg RD 16 AUX_ACK · Reg RD 16 AUX_ACK · Reg RD 10 AUX_ACK · CERT(rx) ·	 16 bytes bytes fro 16 bytes bytes fro 16 bytes bytes fro 10 bytes DPCD Ad 	00 a4 a0 96 91 fb 00 b3 e5 96 92 0b 00 fb 33		Line #179 - 1575444.68ms CERT(rx) - DPCD Address range trace 0x6900b - 0x69214 No extended trace decoding available.
	└─ 🕢 V8-1D	V	180 181 182 183 184 185 186 187 188 189 190 191 192 193 194 195 195 196 197 198 199 200 201 202	1575444,82 1575444,93 1575444,93 1575445,17 1575445,17 1575445,17 1575486,71 1575486,71 1575487,48 1575487,40 1575487,43 1575487,43 1575487,43 1575487,43 1575487,43 1575488,25 1575488,25 1575488,25	Sink HDCP 2.3 Source Sink HDCP 2.3 Source Sink Source Sink Source Sink Source Sink Source Sink Source Sink Source Sink Source Sink HDCP 2.3	Native Native Trace Native Nat	AUX, ACK. R(rx) - DPC Req RD 31 AUX, ACK. Req WR 16 AUX, ACK. Req WR 16 Req Req Req Req Req Req Req Req Req Req	D Addres ytes fro 3 bytes PCD Add 5 bytes to 0 bytes 5 bytes to 1 bytes 5 bytes to 1 bytes 5 bytes to 1 bytes 1 bytes 1 bytes 1 bytes to 1 bytes 1 bytes to 1 bytes 1	00 97 32 96 92 1d 00 02 00 86 92 20 00 86 92 30 00 86 92 40 00 86 92 50 00 86 92 60 00 86 92 70 00 86 92 70 00 86 92 80 00 86 92 90		$\begin{array}{c} - \ \ \ \ \ \ \ \ \ \ $
	Presets	1	<	1575488.94	Jink	Native	AUX_ACK	o bytes	00 >	Ť	DETAILED_CAP_INFO_AVAIL =

DP AUX Analyzer functionality is enabled in UCD-400 by default.

The AUX Analyzer tabs collect AUX Channel Transactions from the Event Log in the *Transaction list*. The user can parse the content of each transaction by clicking the corresponding *transaction line*. The parsed content is in the *Message Details* panel on the right.

Please refer to chapter *Customizing the Main Window* below for details on how to modify the content and look of the *Transaction list*.

Lines

The data is organized in lines, each numbered starting from 1 and marked with a timestamp. There are four kinds of lines:

1. Information lines

Identified by the text "INFO" in their Type column, they provide some useful information like the time acquisition has started and stopped or the logical state of the inputs, etc.

2. Transaction lines

Identified by the text "Native" or "I2C" in their Type column, they report an AUX channel data transfer, either a data Request or a data Reply.

- **3.** Event lines Identified by the text "Event" in their Type column, they signal the state change in one or more of the monitored inputs.
- 4. Sideband Channel Messages The Isochronous Transport Service uses the sideband communications over sideband channel (AUX CH and HPD) for the management of topology/virtual channel connection/Main Link and performs Main Link symbol mapping.

5. Error lines

A line Type reading "Error" marks the detection of an illegal AUX channel data packet. An irregular start condition, an irregular stop condition or transfer of a number of bits which is not a multiple of 8 are all conditions that cause an error line.

6. Trace lines

Combines the data from several lines of a HDCP related message to one entry in *Message details* panel for easier readability.

Columns

The data on each line is ordered in columns. Each column provides additional information about the data line, facilitating its viewing and interpretation:

Line

This column displays the line number, starting from 1, and cannot be hidden.

Timestamp

Each line is identified by its timestamp, marking the instant when an event or error was detected, or when a data transaction got started. The timestamp can be displayed as a time delay from the start of the acquisition (absolute) or from the previous line (relative). The timestamp can be displayed in milliseconds or in minutes, seconds and microseconds.

From

This column indicates the originator of the data line:

- "Source" and "Sink" for an AUX channel transaction, respectively a data Request and a data Reply.
- "Source Trace" and "Sink Trace" respectively for Sideband Message data Request and Reply.
- "DPA-400" for error and information lines.
- "Unknown" for signal state change events.

Туре

This column provides additional information about the type of the line:

- "Native" marks Native AUX channel Requests and Replies.
- "I2C" marks I2C AUX channel Requests and Replies.
- "Sideband Request" and "Sideband Reply" to mark the Sideband Channel messages
- "Event" is used for signal state change events.
- "**INFO**" is used with information lines.
- "Error" is used for illegal conditions detected on the AUX channel.

Details

This column contains an abbreviated description of the line content in textual form.

Data

The binary data exchanged during AUX channel transactions, in hexadecimal notation.

Find

To locate an access to a DPCD location right-click on the list and select **Find...** or select **Ctrl+F** from keyboard. To **Find again** select **F3**.

Search		×
Search for	Any access $~~$ to a	ddr. (Hex):
	🗶 Cancel	Q Search

Message Details

The *Message details* panel is used to provide a detailed explanation of the line currently selected in the *Transaction list*. For AUX channel transaction lines, for each of the DPCD memory locations affected, the panel lists:

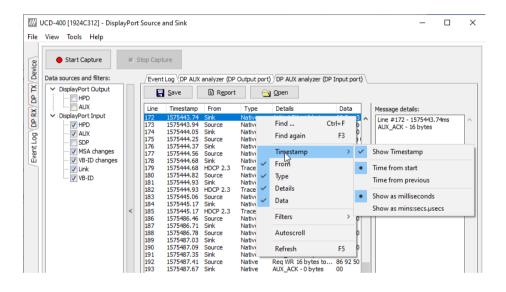
- All data bytes read or written.
- All DPCD memory locations affected.
- The name of the locations and of each of their bit fields.
- All bit field's numeric and binary values, together with their decoded value.
- The Replies outcome (AUX_ACK, AUX_NACK, I2C_DEFER, etc.).

Customizing the Main Window

Format of the data shown in the *Transaction list* and the *Message details* panels can be altered in order to highlight the details of your interest.

Selecting Data Columns

The *Transaction list* can be customized by right-clicking over the list. The pop-up menu allows choosing which columns to display, the style of the timestamp and switch between absolute and relative timestamps. *Filters* limit the transactions shown in the list. Please see *Filtering* later in this document.



Selecting Font and Colors

Select **Tools > Options > AUX Analyzer options** tab. Click **Select new font** and choose the font and size used for displaying the *Transaction list* and the *Message details*.

Options			×
Video, Audio and Misc options AU	X Analyzer options		
Font Selection	Font		×
Select new font Current f	Eont: Tahoma	Regular 1	ize: OOK
Transaction list color option Show / change color settings for	Tahoma TeamViewer12 Tempus Sans ITC Times New Roman	Oblique 1	
Normal item colors	Trebuchet MS	✓ Bold Oblique √ 2	18
Color exar		Sample AaBbYyZz	
Change text color		Sogpt:	
		Western	~
- Highlighted NPCD address r			

Transaction List Color Options

Select the colors for the font and background of various items.

leo, Audio and Misc options AUX Analyzer options	
Font Selection	
Select new font Current font "Tahoma", size 10	
Transaction list color options	
Show / change color settings for:	
Show / change color settings for: Normal item colors	~
	~
Normal item colors Normal item colors Selected item colors	~
Normal item colors Normal item colors Selected item colors Highlighted them colors	~
Normal item colors Normal item colors Selected item colors Highlighted item colors Sideband request message colors	~
Normal item colors Normal item colors Selected item colors Hiphighted item colors Sideband request message colors Sideband request message colors	~
Normal item colors Normal item colors Selected item colors Highlighted item colors Sideband request message colors Sideband reply message colors Sideband reply message colors	~
Normal item colors Normal item colors Selected item colors Hiphighted item colors Sideband repuest message colors Sideband repuyest message colors	~

Highlighted DPCD Address Ranges

In order to improve the readability of the *Transaction list*, you can mark the AUX channel transactions where a certain DPCD register address or address range is highlighted with a color of choice.

Click Add..., select the access type, start DPCD address and end DPCD address of the range in Hex. Click Accept.

Select the range you just created from the **Highlighted DPCD addresses ranges** list and click the **Change test color** and **Change background color** buttons to select the colors desired.

You can create multiple simultaneous coloring rules to help you get a better view of the data captured.

le <u>V</u>	(iew <u>T</u> ools <u>H</u> elp			_				
2	Start Capture		Stop Cap	ture				Options
Device								Video, Audio and Misc options AUX Analyzer options
5 D	ata sources and filters:		/Event	t Log (DP AUX	analyzer (DF	Output po	rt) / DP AUX ana	a Font Selection
≤ ī	✓ · DisplayPort Output			1 Cause	Report		-	
5	HPD			Save	E Report	<u>ا</u>	Open	Select new font Current font "Tahoma", size 10
-	AUX		Line	Timestamp	From	Type	Details	
2	✓ DisplayPort Input		52	1575273.72	Sink	Native	AUX ACK - 1	Transaction list color options
2 5	HPD		52	1575273.91		Native	Reg RD 1 by	
	AUX		54	1575274.02	Sink	Native	AUX ACK - 1	
3	SDP		55	1575274.10	Source	Native	Reg RD 1 by	
			56	1575274.21	Sink	Native	AUX_ACK - 1	Color example for selected item
	MSA changes		57	1575274.28	Source	Native	Req RD 1 by	t Color example for selected item
i	···· 📝 VB-ID changes		58	1575274.38	Sink	Native	AUX_ACK - 1	
hII.	📝 Link		59	1575274.45	Source	Native	Req WR 1 by	
	VB-ID		60	1575274.57		Native	AUX_ACK - 0	
			61	1575274.63		Native	Req RD 6 by	
			62 63	1575274.75 1575274.86	Sink	Native Native	AUX_ACK - 6	Rule #0 - RD/WR from 00050 to 00050
			64	1575274.86	Source	Native	Req WR 1 by AUX ACK - 0	Kule #1 - KD/WK II 0II 00100 to 00107
		<	65	1575275.04		Native	Reg WR 1 by	
			66	1575275.17		Native	AUX ACK - 0	
			67	1575275.22		Native	Reg WR 1 by	
			68	1575275.35	Sink	Native	AUX ACK - 0	
			69	1575275.41	Source	Native	Reg WR 1 by	4
			70	1575275.53	Sink	Native	AUX_ACK - 0	
			71	1575275.59	Source	Native	Req RD 1 by	
			72	1575275.70	Sink	Native	AUX_ACK - 1	
			73	1575275.77	Source	Native	Req WR 1 by	
			74	1575275.89	Sink	Native	AUX_ACK - 0	
			75 76	1575275.96 1575276.16	Source Sink	Native Native	Req WR 5 by	
			77	1575276.32		Native	AUX_ACK - 0 Reg RD 2 by	
			78	1575276.44	Sink	Native	AUX ACK - 2	
			79	1575276.52		Native	Reg RD 2 by	
			80	1575276.65	Sink	Native	AUX ACK - 2	
			81	1575276.74		Native	Reg WR 4 by	
ШL			82	1575276.90	Sink	Native	AUX_ACK - 0	
	Presets	1	<					Edit Custom Filters
	Presets							
								🖌 OK 🛛 🗶 Cancel

Filtering

Transactions lines shown in the transaction list can be limited by *Filtering*. The shown lines can be selected by:

- The type of data line
- The origin of the message
- The DPCD address range

Right click > Filters drop down menu lists a set of pre-programmed filters.

Nat V	Fine Fine	d d again estamp m e ails	- 1 butes Ctrl+F F3 >	001
	Filters >		>	Show HDCP 2.2 Show HDCP 1.3
Nat		resh	F5	Hide Native Hide I2C
Native AUX_ACK - 2 bytes Native Req RD 2 bytes fro Native AUX_ACK - 2 bytes		bytes fro - 2 bytes	Hide Events Hide Errors	
Native Req WR 4 bytes to Native AUX_ACK - 0 bytes			Show Sideband messages only	

Editing Filters

From *Custom Filter* dialog (Tools > Options > Edit Custom Filters ...) allows for adding and modifying filters. The pre-programmed filters are listed in the dialog. Their structure can be copied as bases of your custom filters. It is advisable not to modify the pre-programmed filters directly but make copies of them.

Custo	m Filter					×
Stor	ed custo	m filter defin	itions			
	WHDCP 2					New definition
Hide	Native					Rename selected
	Events					Delete selected
	Errors v Sidebar	nd messages	only			Move Up
		-				Move Down
Filte	r Rules					
Requ	est / Rep	ly Pairing mo	de Auto -	Filter item by request if	reply received within 400µ	us of request \sim
A	Rule	Туре	Source	Range	Comment	
	Show	Native	Src/Sink	0x069000-0x069fff	Show HDCP 2.2. addres	s range
		e da	0	lin David	1	
Ac	ld	Edit	Remove	Up Down		
					X Cancel	🖌 Accept
						•

In the *Stored custom filter definitions* panel, lists currently defined Filters. On the right hand side buttons, you can define new Filters, rename or delete them. Their appearance in the *Filters* pull-down menu can also be altered.

In the *Filter Rules* panel lower in the dialog you can review and change the *Rules* in the selected *Filter*. Add... creates new rules, Edit... enables review and editing existing Filters and **Remove** deletes from the Filter definition.

When clicking Add... or Edit... *Edit Filter Rule* dialog opens. The dialog defines the action of the rule, events and event details.

/// Edit Filter Rule			-		×
Show ~ Native	✓ From Source or Sink		00-0x069fff		
Filter by Data:					
					\sim
					~
Comment (Optional, max 120 chars):	Show HDCP 2.2. address r	ange			
	🔗 Help	X Cancel		🖌 Accep	ot

Click Help to show "Help" text also attached to Appendix F of this document.

Note	Please note that Filters are a very powerful tool. They can however unintentionally hide valuable data from you. Please be careful when applying custom filters. A good practice is to start from an existing filter and gradually add new rules while testing their performance.
Note	Filtering and selecting the columns for display do not affect the actual data acquisition. All transactions and their full data are always captured.

10. EDID EDITOR

UNIGRAF

E-EDID Encoder / Decoder ✓ · Collection 1 Details of ":/0/Version/Vendor _Product ID" Blocks in collection Block 0 [VESA EDID] Kev Value ID Manufacturer Nam UFG ✓ · Version ID Product Code 0x4036 Extension flag ID Serial Number 0x3032344 Extension flag Vendor & Product ID Basic Display Parameters and F Display x,y Chromacity coordin Manufacture or Model year Manufacture Year and Week Established timings I and II Manufacturer's Timings Week of manufacture Week 52 Standard Timings 18-Byte data blocks Year of manufacture Year 2014 Descriptor 1 Descriptor 2 Descriptor 3 > · Descriptor lock 1 [CEA 861] Checksum CEA Extensions Version nk Underscans IT video Basic audio YCbCr (4:4:4) Save Show Hex 🕵 Show Log 🕞 Load

The EDID Editor main window is divided into three logical areas. The bottom part of the

window contains the command buttons, and the log view. The top-left portion shows the currently edited E-EDID blocks in a tree-form, and the top-right portion shows an edit control for the currently selected item, possibly a list of sub-keys and their names (The list is not shown for all values) and the HEX-view of the block collection.

Command Buttons

Load: Load an EDID block collection file from disk. Save: Save the current block collection to a disk file. Show Hex: Show or Hide the HEX view. Show Log: Show or Hide the Log view.

EDID Editor Features

The EDID Editor currently supports VESA E-EDID block versions 1.3 and 1.4. As the standard defines, the versions 1.0, 1.1 and 1.2 are supposed to be backward compatible, and therefore the VESA E-EDID decoder will also show their contents. However, in these cases it should be noted that the error checking is not compliant with restrictions given in these older versions of the standard. In addition to VESA E-EDID block, the CEA-861 versions 1, 2 and 3 EDID blocks are also fully supported as well as the VESA Block Map Extension blocks.

Practically unlimited number of extension blocks may exist in a single collection. The number of blocks is limited by VESA Specifications and possibly by available system resources. Most EDID blocks contain a structure that is very similar to a tree-structure. The EDID Editor decodes each block into a tree-view of the block. The tree-view then contains all values contained within the EDID block. The contents can then be easily browsed, using only a few mouse clicks. The EDID Editor has a support for automatic variables, such as the block checksum. When the user changes a value in an EDID block, the tool will update the checksum accordingly. The automatic variables appear as read only values for the user. A log print will be made when an automatic variable is updated by the editor.

HEX View: An optional HEX data display of all blocks in the collection. The view also shows the latest changes highlighted.

LOG View: An optional LOG view, which will contain log prints generated by the editor. Mostly it will list values that have been automatically updated due to edits.

Editing Tips

Editing an EDID block is very straightforward, but there are some special cases where the user must know how to accomplish certain types of tasks.

- Enter key will apply text-edit values and combo-box selection.
- To apply new setting to *binary* values (ones that show a check-box), please click the **Set** button.
- When you see a **Quick Config** button appear below an editor, you can access a configuration menu that allows you to quickly select one of multiple pre-defined setup options.
- In CEA-861 blocks, you can add and remove 18-byte descriptors and CEA data blocks by setting the values "18-byte Descriptors in this block" and "CEA Data block count". Unfortunately re-arranging the descriptors and CEA data blocks is not supported yet, so you need to be careful when editing these.
- Enter hex values with prefix "0x" or "\$", no prefix means a decimal value.
- You can always enter HEX or DEC, even if the value is presented as HEX, and/or value range is given in HEX.
- Floating point values must be given with period "." as decimal separator, even if your localization setting defines decimal separator as comma (or other).
- Remember to click **Set** after changing a bit-value presented as a single check-box if you want the new value applied.

Note It is recommended that you back up the un-edited EDID contents to a file before editing and writing it to the card.

Saving EDID Data

When you are done with editing you can either save the EDID contents to a file in the PC or bring it in the *HEX Editor*.

For saving the data to a file in your PC click Save.

For bringing the data to the HEX Editor close the EDID Editor window by clicking the **Window Close** button in the top right-hand corner of the window. You will be asked if you would like to copy and replace the EDID data in the HEX Editor. Click **Yes** to replace the data, click **No** to discard the modifications.

When you are back in the *HEX Editor*, the bytes that the *EDID Editor* changed are highlighted with **BLUE BACKGROUND**.

APPENDIX A. PRODUCT SPECIFICATION

UCD-400

Input	DisplayPort™ 1.4a compliant (DP Rx)
Output	DisplayPort™ 1.4a compliant (DP Tx)
Max video mode	7680 × 4320 p30 input and output 3840 × 2160 p120 input and output
Audio	LPCM, 2 – 8 channels, 44.1 to 192 kHz
Content Protection	HDCP 2.3, HDCP 1.3
DSC Capability	DSC sink with off-line decompression DSC source using pre-compressed content
Additional features	FEC, LTTPR*, DSC* DP 1.4a LL CTS*, DP DSC CTS* HDCP 2.3 CTS*
Computer interface	USB 3.0
Software	Windows 10, 8 and 7 compatible software drivers, UCD Console application for Windows. Compatible with Unigraf TSI SDK.
Power supply	AC/DC Power supply (100 to 240 Vac 50/60 Hz input, +12 Vdc output)
Mechanical Size	280 × 200 × 80 mm
Weight	1.2 kg w/o power supply

*) Please contact Unigraf for detailed availability

APPENDIX B. LICENSING

In the following pages, please find detailed explanation of the functions and the licensing. Please refer to TSI documentation on detailed description of TSI features.

DisplayPort Reference Sink (DPRX)

				-		
Тар	Function	Basic	DSC Decoder	DP 1.4a LL CTS for testing Source DUT	HDCP 2.3 CTS for testing Source DUT	HDCP 2.3 CTS for testing Repeater DUT
Video						
	Preview, Capture, Snap preview	•				
	Status	•				
Audio		•				
	Monitor, Capture and graphical preview	•				
	Status	•				
Link		•				
	Link Status, Link Configuration	•				
	Stream Status (video, audio)	•				
	HPD Status, HPD Assert / De-assert, HPD Long Pulse, HPD Short Pulse	•				
	MST Feature (up to 4 streams)	•				
	FEC Feature	•				
	DSC Decoder					
EDID						
	Read / Write, Save / Load, EDID Editor	•				
DPCD						
-	Read/Write, Save/Load	•				
	DPCD Decoder	•				
HDCP						
-	HDCP 1.3 and HDCP 2.3 Support	•				
	Authentication status, Encryption status	•				
Event Log						
<u>J</u>	Event Log	•				
	DP AUX Analyzer	•				
Source DUT Testing						
<u> </u>	Execute TSI Tests	•				
	Execute DP LL CTS					
	Execute Audio CTS					
	Execute FEC CTS					
	Execute DSC CTS					
	HDCP 2.3 CTS for testing DP Source DUT					
	HDCP 2.3 CTS for testing DP Repeater DUT					

DisplayPort Reference Source (DPTX)

Tab	Function	Basic	DSC Encoder	LTTPR	DP 1.4a LL CTS for testing Sink DUT	HDCP 2.3 CTS for testing Sink DUT	HDCP 2.3 CTS for testing Repeater DUT
Pattern Generator							
	Fixed and custom Video Timings	٠					
	Fixed and custom Video Patterns	•					
Audio Generator							
	Play audio files	•					
Link							
	Link Status	•					
	HPD Status: (Asserted / De-asserted)	•					
	Link Configuration: (Lane count, Link Rate, Framing mode, Clock mode)	•					
	MST Feature (up to 4 streams)	•					
	FEC Feature	•					
	DSC Encoder						
	LTTPR Feature						
EDID							
	Read / Write, Save / Load, EDID Editor	•					
DPCD							
	Read / Write, Save / Load	•					
	DPCD Decoder	•					
HDCP							
	HDCP 1.3 Support	•					
	Control: (Enable / Disable, authenticate only, Encryption Enable / Disable)	•					
	Status: (Authentication status, Encryption status)	•					
	HDCP 2.3 Support	•					
Event Log							
	Event Log	٠					
	DP AUX Analyzer	•					
Sink DUT Testing							
	Execute TSI Tests	•					
	Execute DP LL CTS						
	Execute Audio CTS						
	Execute FEC CTS						
	Execute DSC CTS						
	HDCP 2.3 CTS for testing DP Sink DUT						
	HDCP 2.3 CTS for testing DP Repeater DUT						

APPENDIX C: PREDEFINED TIMINGS

Description	H active	V active	H total	V total	Frame rate	RGB 6 bpc	RGB 8 bpc	RGB 10 bpc	RGB 12 bpc	RGB 16 bpc
VESA 800 x 600 @ 60Hz	800	600	1056	628	60	•	•	•	•	•
VESA 848 x 480 @ 60Hz	848	480	1088	517	60	•	•	•	•	•
VESA 1024 x 768 @ 60Hz	1024	768	1344	806	60	•	•	•	•	•
CTA 1280 x 720 @ 60Hz	1280	720	1650	750	60	•	•	•	•	•
VESA 1280 x 768 @ 60Hz	1280	768	1664	798	60	•	•	•	•	•
VESA 1280 x 960 @ 60Hz	1280	960	1800	1000	60	•	•	•	•	•
VESA 1280 x 800 @ 60Hz [RB]	1280	800	1440	823	60	•	•	•	•	•
VESA 1280 x 800 @ 60Hz	1280	800	1680	831	60	•	•	•	•	•
VESA 1280 x 768 @ 60Hz	1280	768	1440	790	60	•	•	•	•	•
VESA 1280 x 1024 @ 60Hz	1280	1024	1688	1066	60	•	•	•	•	•
VESA 1360 x 768 @ 60Hz	1360	768	1792	795	60	•	•	•	•	•
VESA 1400 x 1050 @ 60Hz	1400	1050	1560	1080	60	•	•	•	•	•
VESA 1600 x 1200 @ 60Hz [RB]	1600	1200	1760	1235	60	•	•	•	•	•
VESA 1600 x 1200 @ 60Hz	1600	1200	2160	1250	60	•	•	•	•	•
VESA 1680 x 1050 @ 60Hz	1680	1050	2240	1089	60	•	•	•	•	•
VESA 1680 x 1050 @ 60Hz [RB]	1680	1050	1840	1080	60	•	•	•	•	•
VESA 1792 x 1344 @ 60Hz	1792	1344	2448	1394	60	•	•	•	•	•
VESA 1920 x 1080 @ 30Hz [RB1]	1920	1080	2080	1096	30	•	•	•	•	•
VESA 1920 x 1080 @ 30Hz [RB2]	1920	1080	2000	1096	30	•	•	•	•	•
CTA 1920 x 1080 @ 30Hz	1920	1080	2200	1125	30	•	•	•	•	•
VESA 1920 x 1080 @ 60Hz [RB1]	1920	1080	2080	1111	60	•	•	•	•	•
VESA 1920 x 1080 @ 60Hz [RB2]	1920	1080	2000	1111	60	•	•	•	•	•
CTA 1920 x 1080 @ 60Hz	1920	1080	2200	1125	60	•	•	•	•	•
VESA 1920 x 1080 @ 120Hz [RB1]	1920	1080	2080	1144	120	•	•	•	•	•
VESA 1920 x 1080 @ 120Hz [RB2]	1920	1080	2000	1144	120	•	•	•	•	•
CTA 1920 x 1080 @ 120Hz	1920	1080	2200	1125	120	•	•	•	•	•
VESA 1920 x 1440 @ 60Hz	1920	1440	2600	1500	60	•	•	•	•	•
VESA 2048 x 1536 @ 60Hz	2048	1536	2208	1580	60	•	•	•	•	•
VESA 2560 x 1440 @ 60Hz	2560	1440	2720	1481	60	•	•	•	•	•
VESA 2560 x 1080 @ 60Hz	2560	1080	3424	1120	60	•	•	•	•	•
VESA 2560 x 1080 @ 60Hz [RB]	2560	1080	2720	1111	60	•	•	•	•	•
VESA 2560 x 1600 @ 60Hz	2560	1600	3504	1658	60	•	•	•	•	•
VESA 2560 x 1600 @ 60Hz [RB]	2560	1600	2720	1646	60	•	•	•	•	•
Other 2880 x 1440 @ 60Hz	2880	1440	2976	1456	60	•	•	•	•	•

• = Supported video mode and color depth (without DSC)

Description	H active	V active	H total	V total	Frame rate	RGB 6 bpc	RGB 8 bpc	RGB 10 bpc	RGB 12 bpc	RGB 16 bpc
VESA 4096 x 2160 @ 60Hz	4096	2160	4176	2222	60	•	•	•	•	
VESA 3840 x 2160 @ 30Hz [RB1]	3840	2160	4000	2191	30	•	•	•	•	•
VESA 3840 x 2160 @ 30Hz [RB2]	3840	2160	3920	2191	30	•	•	•	•	•
CTA 3840 x 2160 @ 30Hz	3840	2160	4400	2250	30	•	•	•	•	•
CTA 3840 x 2160 @ 50Hz	3840	2160	5280	2250	50	•	•	•	•	
CTA 4096 x 2160 @ 50Hz	4096	2160	5280	2250	50	•	•	•	•	
VESA 3840 x 2160 @ 60Hz [RB1]	3840	2160	4000	2222	60	•	•	•	•	•
VESA 3840 x 2160 @ 60Hz [RB2]	3840	2160	3920	2222	60	•	•	•	•	•
CTA 3840 x 2160 @ 60Hz	3840	2160	4400	2250	60	•	•	•	•	
CTA 4096 x 2160 @ 60Hz	4096	2160	4400	2250	60	•	•	•	•	
VESA 3840 x 2160 @ 120Hz [RB1]	3840	2160	4000	2287	120	•				
VESA 3840 x 2160 @ 120Hz [RB2]	3840	2160	3920	2287	120	•	•			
CTA 3840 x 2160 @ 120Hz	3840	2160	4400	2250	120	•				
VESA 5120 x 2160 @ 30Hz [RB1]	5120	2160	5280	2191	30	•	•	•	•	•
VESA 5120 x 2160 @ 30Hz [RB2]	5120	2160	5200	2191	30	•	•	•	•	•
CTA 5120 x 2160 @ 30Hz	5120	2160	6000	2200	30	•	•	•	•	•
VESA 5120 x 2160 @ 60Hz [RB1]	5120	2160	5280	2222	60	•	•	•	•	
VESA 5120 x 2160 @ 60Hz [RB2]	5120	2160	5200	2222	60	•	•	•	•	
CTA 5120 x 2160 @ 60Hz	5120	2160	5500	2250	60	•	•	•		
VESA 5120 x 2160 @ 120Hz [RB1]	5120	2160	5280	2287	120					
VESA 5120 x 2160 @ 120Hz [RB2]	5120	2160	5200	2287	120	•				
CTA 5120 x 2160 @ 120Hz	5120	2160	5500	2250	120					
Other 5120 x 2880 @ 60Hz	5120	2880	5280	2962	60	•	•			
VESA 7680 x 4320 @ 30Hz [RB1]	7680	4320	7840	4381	30	•	•			
VESA 7680 x 4320 @ 30Hz [RB2]	7680	4320	7760	4381	30	•	•			
CTA 7680 x 4320 @ 30Hz	7680	4320	9000	4400	30	•				
VESA 7680 x 4320 @ 60Hz [RB1]	7680	4320	7840	4443	60					
VESA 7680 x 4320 @ 60Hz [RB2]	7680	4320	7760	4443	60					
CTA 7680 x 4320 @ 60Hz	7680	4320	9000	4400	60					
VESA 7680 x 4320 @ 100Hz [RB1]	7680	4320	7840	4529	100					
VESA 7680 x 4320 @ 100Hz [RB2]	7680	4320	7760	4529	100					
CTA 7680 x 4320 @ 100Hz	7680	4320	10560	4500	100					

• = Supported video mode and color depth (without DSC)

APPENDIX D: PREDEFINED PATTERNS

Selection	Pattern	Description
Disabled	N/A	The links are activated but no video data transferred
Color Bar		100% intensity color bars of all primaries and mixed combinations.
Chessboard		8 by 8 chessboard with black (0%) and 100% intensity white
Solid Black		0% luminance
Solid White		100% white
Solid Red		100% red
Solid Green		100% green
Solid Blue		100% blue
White Vertical Stripes		Vertical stripes of black (0%) and white (100%). Parameters set the widths of the black and white stripes in pixels respectively. Default black / white = 20 / 20 pixels. Parameter range 0 to 5000.
Gradient Vertical Stripes		16 pixels high horizontal red green, blue and white stripes. Intensity is increased from 0 to 100% with steps defined by the given parameter (n). (step = n*color_depth/256). "n" range 0 to 5000 (default 120).
Color Ramp		Color Ramp test pattern defined by VESA DisplayPort Link Layer Compliance Test Specification.
Color Square		Color Square test pattern defined by VESA DisplayPort Link Layer Compliance Test Specification. Color mode can be selected between RGB, YCbCr 4:4:4, 4:2:2, 4:2:0 (ITU Rec 601 / 709)
Motion Pattern		Horizontally moving color bar pattern. The pattern is shifted to left one pixel in each frame in a sequence. The length of the sequence is defined with parameter. Range 0 to 34 (default is 20)
Custom Image	UNICEAF	Bitmap image uploaded by the user. Click on the Custom Images panel to browse. By default, Unigraf test image will be used.

More test patterns can be downloaded e.g. from www.icdm-sid.org/downloads/testpatterns.html.

APPENDIX E: SINK, SOURCE AND REPEATER DUT TESTS

The tables below list the Unigraf TSI SDK Test Cases that you can run in *Sink DUT Testing / Source DUT Testing* tabs of UCD Console, their definition in *TSI Reference Manual* and the licensing needed.

Source DUT Testing		Default	DP 1.4a LL CTS*	DP HDCP 2.3 CTS*
CRC based Video Test Set				
	CRC based single frame reference video test (TSI TEST VIDEO CRC SINGLE REF)	✓		
	CRC based single frame stability test (TSI TEST CRC VIDEO STABILITY)	✓		
	CRC based sequence of frames reference video test (TSI TEST CRC VIDEO SEQUENCE)	✓		
	CRC based continuous sequence of frames reference video test (TSI_TEST_CRC_CONT_VIDEO_SEQUENCE)	√		
Link Test Set				
	Link Training at All Supported Lane Counts and Link Rates (TSI_TEST_DP_SIMPLE_LINK)	✓		
DP 1.4a Link Layer CTS				
	4.2.1.1 – 4.2.1.5, 4.2.2.1 – 4.2.2.10, 4.3.1.1 – 4.3.1.13, 4.3.2.1 – 4.3.2.5 4.3.3.1, 4.4.1.1 – 4.4.1.3, 4.4.2, 4.4.3, 4.4.4.1 – 4.4.4.6, 4.5.1.1 – 4.5.1.2, 4.6.1.1 – 4.6.1.9		~	
HDCP 2.3 CTS 1A Test Set	HCDP2.3 CTS 1A-01 – HCDP2.3 CTS 1A-13			<
HDCP 2.3 CTS 1B Test Set	HCDP2.3 CTS 1B-01 – HCDP2.3 CTS 1B-10			 Image: A second s

Sink DUT Testing		Default	DP 1.4a LL CTS*	DP HDCP 2.3 CTS*
DP 1.4a Link Layer CTS				
	5.2.1.1 – 5.2.1.12, 5.2.2.1 – 5.2.2.9, 5.3.1.1 – 5.3.1.9, 5.3.2.1 – 5.3.2.2, 5.4.1.1 – 5.4.1.4, 5.4.2, 5.4.3.1 – 5.4.3.2, 5.4.4.1 – 5.4.4.6, 5.5.1.1 – 5.5.1.7, 5.6.1.1. – 5.6.1.26, 5.6.2.1 – 5.6.2.14		>	
HDCP 2.3 CTS 2C Test Set	HCDP2.3 CTS 2C-01 – HCDP2.3 CTS 2C-06			 Image: A set of the set of the

Repeater DUT Testing		Default	DP HDCP 2.3 CTS*	
HDCP 2.3 CTS 3A Test Set	HCDP2.3 CTS 3A-01 – HCDP2.3 CTS 3A-06		 Image: A set of the set of the	
HDCP 2.3 CTS 3B Test Set	HCDP2.3 CTS 3B-01 – HCDP2.3 CTS 3B-07		 Image: A set of the set of the	
HDCP 2.3 CTS 3C Test Set	HCDP2.3 CTS 3C-01 – HCDP2.3 CTS 3C-25		 Image: A set of the set of the	

*) Separate licenses for testing Sink, Source, Branch (LL CTS) and Repeater (HDCP) DUT

CRC Based Video Test Set – DP RX

CRC Based Single Reference Frame Video Test

The test compares captured frames to a provided reference.

TE compares the video mode (Frame Width, Height, BPP and optionally Frame rate) to provided parameters and after that captures frames and compares the CRC (check sum) of their three color components to the provided reference until the number of bad frame limit provided is detected or the provided total number of frames is reached.

The test is judged FAIL if video mode does not match or the number of bad frames is exceeded.

The test optionally captures the failed frames as bitmap images and stores them into the hard disc.

Parameters in use

- Test Timeout (default 100 000 ms)
- Total number of frames (default 2 000 ms)
- Number of bad frames allowed (default 2)
- Reference width (default 1920)
- Reference height (default 1080)
- Reference BPP (default 24)
- Expected frame rate (mHz)
- Frame rate tolerance (mHz)
- Reference CRCs (R, G, B)

CRC Based Single Frame Video Stability Test

The test verifies that the captured video is stable.

TE captures a frame and sets the CRC of its color components as reference. After that TE captures frames and compares their CRC (check sum) to the reference until the number of bad frame limit provided is detected or the provided total number of frames is reached.

The test is judged FAIL if the number of bad frames is exceeded.

The test optionally captures the failed frames as bitmap images and stores them into the hard disc.

Parameters in use

- Test Timeout (default 100 000 ms)
- Total number of frames (default 2 000 ms)
- Number of bad frames allowed (default 2)

CRC Based Sequence of Reference Frames Test

The verifies that a sequence of frames is captured in the right order.

TE compares the video mode (frame Width, Height, BPP and optionally Frame rate) to provided parameters. After that captures frames to find a frame with matching CRC (check sum) of their three color components to the first provided reference. After the first matching CRC is found it compares the CRC of the following frames until the Number of frames tested parameter is reached.

The test is judged FAIL if video mode does not match, the first frame in the list is not found or the CRC of the following frames do not match the provided list.

The test optionally captures the failed frames as bitmap images and stores them into the hard disc.

Parameters in use

- Test Timeout (default 100 000 ms)
- Number of frames to be tested (default 20)
- Reference width (default 1920)
- Reference height (default 1080)
- Reference BPP (default 24)
- Expected frame rate (mHz)
- Frame rate tolerance (mHz)
- Reference CRCs (R, G, B)

Note: Please note that in order for the TE to maintain the sequence, all CRCs in the reference frame list should be different.

CRC Based Continuous Sequence of Reference Frames Test

The test verifies that a sequence of frames is captured in the right order many times repeatedly.

TE compares the video mode (frame Width, Height, BPP and optionally Frame rate and Color format) to provided parameters. After that captures frames to find a frame with matching CRC (check sum) of their three color components to the first provided reference. After the first matching CRC is found it compares the CRC of the following frames until the Number of frames tested parameter is reached. After that it resets the list and starts from the first CRC. The list is repeated until timeout or until the provided number of repetitions is reached.

The test is judged FAIL if video mode does not match, the first frame in the list is not found or the CRC of the following frames do not match the provided list.

The test optionally captures the failed frames as bitmap images and stores them into the hard disc.

Parameters in use

- Test Timeout (default 100 000 ms)
- Number of frames to be tested (default 20)
- Number of iterations
- Reference width (default 1920)
- Reference height (default 1080)
- Reference BPP (default 24)
- Expected frame rate (mHz)
- Frame rate tolerance (mHz)
- Expected color format
- Reference CRCs (R, G, B)

Note: Please note that in order for the TE to maintain the sequence, all CRCs in the reference frame list should be different.

Link Test Set – DP RX

Link Training at All Supported Lane Counts and Link Rates

Test requests link training on all supported lane counts and link rates. Each link training must be successfully completed in order to pass the test.

Parameters in use

- Test Timeout (default 5 000 ms)
- Max lane count supported by DUT (default 4)
- Max lane rate supported by DUT as multiple of 0.27 Gbps. (valid settings 6, 10 and 20; default 20)
- Long HPD pulse duration (default 1 000 ms)
- Link training start timeout (default 5 000 ms)
- Delay between test cycles (default 3 000 ms)

APPENDIX F: ADVANCED FILTERS

This the description of the advanced methods for filtering transactions in *DP AUX analyzer* in *Event Log*. The following help text can be seen as well by clicking the Help button of the *Edit Filter Rule* dialog.

Note Please note that Filters are a very powerful tool. They can however unintentionally hide valuable data from you. Please be careful when applying custom filters. A good practice is to start from an existing filter and gradually add new rules while testing their performance.

Note Filtering and selecting the columns for display do not affect the actual data acquisition. All transactions and their full data are always captured.

Data pattern expressions

A data-pattern expression is a string that describes how to determine if a data-block should be considered as "matched" or "unmatched". The syntax used with data-pattern expressions in Aux Channel Analyzer is described below

The data-block must be covered completely by the data-pattern expression. If the data block is shorter, or longer than the expression, then the data block is determined as "not matched". The '*' wildcard can be used to allow data blocks of any size to match.

Whitespaces and new-lines are ignored and are allowed anywhere; White spaces and new-lines can be used strategically to make the expression more readable.

For example: "*!(10)??(10)" is the same as "* ! (10) ? ? (10)"

Comment blocks:

Comments must be written enclosed in curly-braces '{' and '}'.

Wildcards

Wildcards used are '*' and '?'

? = Match any single data byte only.

* = Match any number of any data bytes. (including the possibility of matching NO data bytes)

For data matching, the byte value must be enclosed in braces '(' and ')'. Use prefixes '\$' to indicate HEX value, '%' to indicate BIN. No prefix indicates DEC.

Examples:

* (\$10) (\$00) : Matches any data pattern that has the bytes \$10, \$00 at end of data.

? (\$10) (\$00) : Matches 3-byte data pattern that has \$10 as second byte and \$00 as third byte.

* (\$10) * (\$00) : Matches any data pattern that has \$10 and ending to a \$00 byte.

* (\$10) * (\$00) *: Matches any data pattern that has \$10 and \$00 after it.

(\$10) ? * (\$20) * : Matches any data pattern that has \$10 as first byte, followed by \$20 with at least one other byte in between. (i.e. will not match \$10, \$20)

Use '!' to invert the match:

!(\$00) = Match any data byte that isn't \$00.

Use '?' within HEX or BIN value to ignore that bit in comparison:

(\$??) = ? = Any data Byte.

(\$?0) = Any data byte with bits 0-3 cleared.

(%1??????) = Any data byte with bit 7 set.

(%0?????1) = Any data byte with bit 7 cleared and bit 0 set.

The '!' inversion can still be used:

!(%?????00) = Matches any data byte ending to %10, %11, %01 but not %00.

To match a single data byte with more than one value, separate the values with comma ',':

(0, 1, 100, 200, 254): Matches a data byte whose value is 0, 1, 100, 200 or 254.

Invert the value group match with '!'. Value wildcard '?' is also allowed.

Example:

!(1, 2, 3): Match any data byte other than 1, 2 or 3.

!(\$?f, \$f?): Don't match data bytes with bits 0-3 set to 1, or data bytes that have bits 7-4 set.